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A three terminal (transistor-like) photodetector fabricated on a silicon-on-insulator substrate with a high responsivity over a wide spectral range from ultraviolet to the near infrared is described. Even for low gate and drain voltages of −0.15 V and +1 V, respectively, its responsivity is 0.5 A/W at 315 nm, 0.63 A/W at 455 nm, and 0.26 A/W at 880 nm. Moreover, the device exhibits a negative differential resistance (due to Pt nano particles which are embedded within the gate dielectric) with large peak-to-valley current ratios of 60 in the dark and up to 140 under illumination. These values are several times larger than those obtained in alternative two or three terminal systems which are based on heterostructures or structures with extremely high doping regions that cause band-banding or resonant tunneling. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4954699]

Multi-functional optically sensitive devices based on the dielectric stacks with embedded metal nano particles (NP) fabricated on silicon–on–insulator (SOI) substrates have been researched extensively in recent years.[1–3] These simple, CMOS compatible elements exhibit a variety of functionalities including illumination dependent nonvolatile memory[1] highly sensitive photodetectors,[2,3] and widely tunable optical varactors.[3]

The various devices are all two terminal elements where additional functions, mainly logic or nonlinear electronic characteristics, are not possible. Widening the functional scope of this family of simple devices requires, therefore, the use of three terminal (transistor-like) structures which should, however, remain simple while maintaining high quality performance.

In this paper, we introduce a three terminal device which maintains the superb optical response of previous two terminal devices but adds the important function of negative differential resistance (NDR). This nonlinear effect is controllable by vertical (gate-source) and the lateral (source-drain) voltages as well as by the illumination intensity. The lateral electrodes are called "source" and "drain," in analogy with field effect transistor (FET) terminology. The vertical (gate) voltage is used to modulate the channel carrier density and thereby control the current-voltage characteristics between the source and drain regions. NDR is widely used in oscillators[4] memory[5] and logic[6] circuits and controlling it optically adds an important degree of freedom for many applications.

Fig. 1 shows a schematic structure of the three terminal device. A SOI substrate with a 2.8 μm thick, 90 Ωcm, N-type device layer is covered by a dielectric stack comprising a 2.8 nm SiO_2 and a 20 nm HfO_2 layers with Pt NPs embedded between them. The Pt NP were fabricated by a low temperature atomic layer deposition process *in-situ* with the HfO_2.film. A pair of metallic electrodes deposited directly on the silicon device layer without any local doping form the drain and source.[7] The gate, source, and drain electrodes are stacks of Ti/Pt/Al. Devices with no Pt NPs were also fabricated and tested for comparison. The channel width and length are, respectively, 25 μm and 20 μm while the gate-source and gate drain distances are 5 μm. The optical characterization used a light emitting diode array in the 315–880 nm wavelength range. The illumination spot area was 1.55×10^{-6} cm^2, while the area of the optical window was 2.65×10^{-6} cm^2.

The source electrode was grounded so that all the voltage levels stated throughout the text are referenced to its (zero) potential. The current-voltage characteristics were measured in the drain and gate voltages (V_D and V_G, respectively) range of −3 V to +3 V using 30 mV increments and a delay time of 80 μs. An Agilent 4155C semiconductor parameter analyzer in the FET mode with a grounded source was employed for the characterization.

The NDR characteristics are highlighted in Fig. 2 which shows the transfer (I_D-V_G) characteristics for different V_D values. Figs. 2(a) and 2(b) describe the case of a negative drain voltage. Double valley shaped NDR curves are exhibited, with peak values that increase with the absolute value of the negative drain voltage. Under illumination, the NDR is significantly amplified. The transfer characteristics at low gate voltages (where $|V_G|$ is less than that yielding the NDR peak) are similar to those of a p-channel depletion mode MOS FET.[8] Figs. 2(c) and 2(d) reveal that a weak degree of NDR (see red and blue arrows) is present also for a positive drain voltage, mainly under illumination. At large positive $V_{D,}$ the valleys converge to plateau regions (see green arrows) which shift to the negative V_G side. The same is true

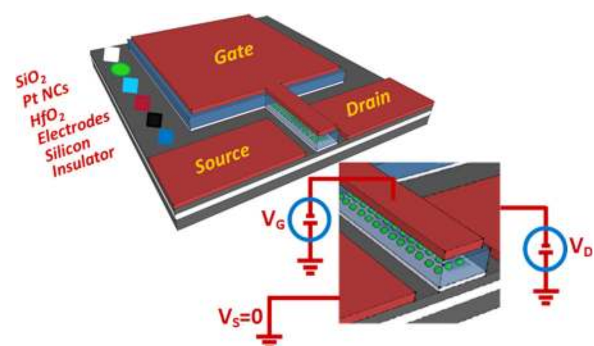

FIG. 1. A schematic structure of the three terminal device based on SOI.

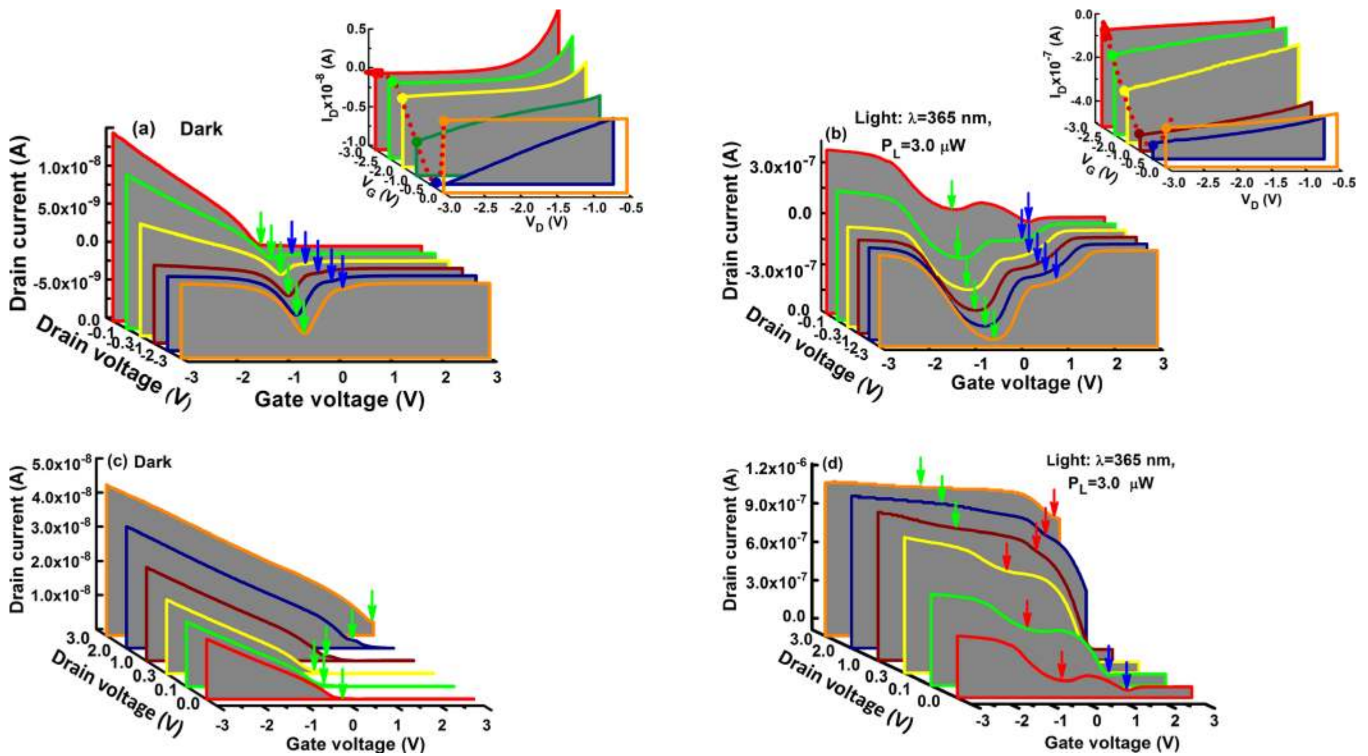

FIG. 2. Transfer characteristics in the dark (a) and (c); under illumination (b) and (d) of structures containing Pt NPs. Arrows indicate the peaks and bends in the I_D-V_G curves. The insets show the output characteristics at negative V_D and V_G.

for the output (I_D–V_D) characteristics under negative drain and gate voltages, which are shown in the insets of Figs. 2(a) and 2(b). The clear NDR nature is seen in the insets, when the dependence of the I_D-V_D characteristic on the gate voltage, illustrated by the trajectory shown by a broken line. At negative V_D and for $|V_G| \geq 0.5$ V, the output characteristics are super linear in the dark and linear under illumination. At $|V_G| \leq 0.5$ V, saturation is observed in both regimes. Thus, at negative drain voltages, the I_D-V_D curves resemble somewhat a p-channel depletion mode MOS FET in the triode regime, in particular, under illumination.

Dependences on illumination intensity are described in Fig. 3. Fig. 3(a) shows the I_D dependence on illumination for a drain voltage of zero while Fig. 3(b) shows the same data for $V_D = -1$.

There are several known device and mechanisms leading to a current-voltage characteristic with a NDR nature. One is quantum mechanical band-to-band tunneling in degenerately doped p-n junction diode.[9,10] NDR is also commonly observed in resonant tunneling through the double-barrier in hetero structures diodes where energy band overlap enhances the tunneling probability.[11,12] Single electron tunneling devices[13] also exhibit NDR. None of these mechanisms is feasible in the present devices which have a long, undoped channel. Other potential mechanisms, which are also unlikely, include hot electrons created in the narrow inversion channel or drain-channel regions (due to the pinch-off effect[14]) whose creation requires electric fields[12] larger than 1 MV/cm and a doping level, above 1×10^{18} cm^{-3}. Finally, self-heating due to power dissipation in the channel[15] is also not relevant in the present case. The lateral electric field under the conditions where NDR is observed is

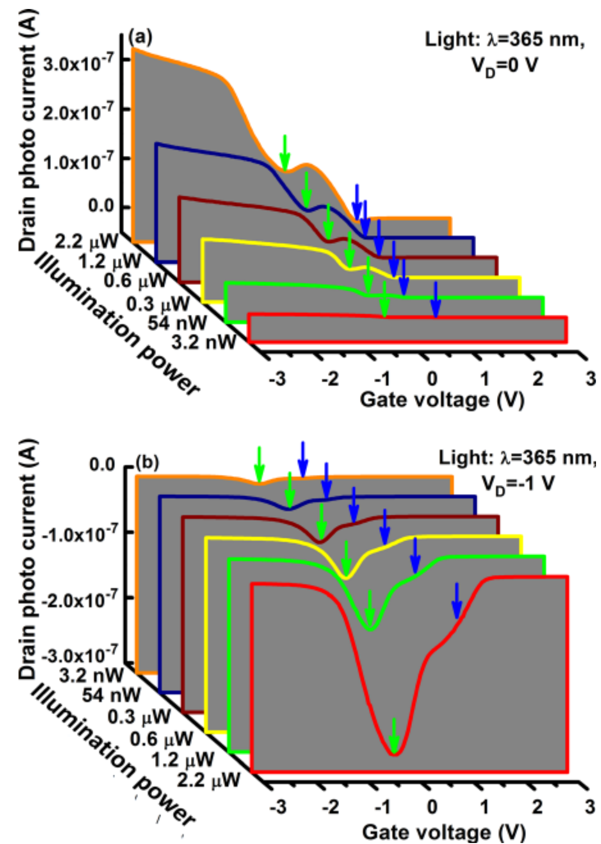

FIG. 3. Transfer characteristics dependence on illumination at 365 nm measured at $V_D = 0$ V and $V_D = -1$ V in a structure containing Pt NPs. Arrows indicate the movement of the extremal points: peaks and bends with illumination power.

approximately 2×10^3 V/cm while the corresponding vertical field is 2×10^5 V/cm. These values cannot initiate the self-heating process.

It was shown in Ref. 16 that when the gate insulator includes charge trapping sites, placed close to the FET channel region, NDR type I_D-V_D characteristics is induced. Similar characteristics were observed in non-volatile memory FET transistors[17] based on the bulk Si with Pt NP trap sites embedded between ultrathin SiO_2 tunneling and HfO_2 blocking layers of the gate insulator stack. We conclude, therefore, that the observed NDR phenomenon is indeed induce by carrier occupation of traps states within gate dielectric stack. In current devices, the NDR effect does not emanate only from the Pt nanoparticle sites (as in Ref. 17) or interfacial trap states (as in Ref. 16) since structures with Pt NPs that have not undergone the voltage stress process as well as voltage stressed structures that lack Pt NPs do not reveal any such NDRs. The last statement is supported by the I_D-V_G curves of structures without Pt NPs, shown in Fig. 4. It can be clearly seen that independent of illumination regimes and V_G or V_D polarities the I_D-V_G curves do not include NDR type non-monotonic dependences. Thus, the existence of the filament-type leakage paths[2,3] in the gate dielectric stack is imperative to ensure penetration of the channel carriers and their trapping on the Pt NPs.

The appearance of double valley shaped NDR (peaks or plateaus) at different gate voltages and their shift can be related to a trapping process of channel carriers by non-uniform size distributed Pt NPs.[3] The ability of large sized NPs to be charged with number of carriers greater than small ones is the known effect due to size dependent Coulomb energy gap (ΔE_g).[18] Values of ΔE_g increase and thus the number of trapped carriers reduces proportionally with the

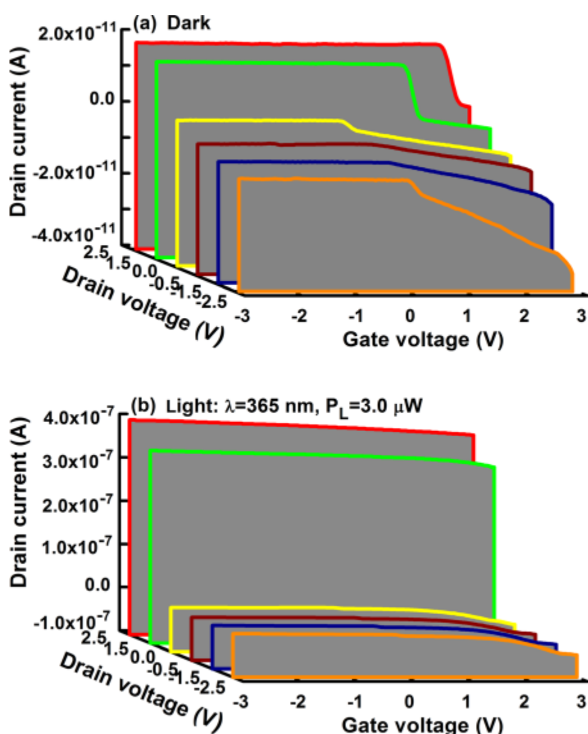

FIG. 4. Transfer characteristics in the dark (a) and under illumination (b) of a structure without Pt NPs.

NPs size reduction. However, revealed low drain current plateau region (and not peak, which would indeed require the existence of another main group of small sizes NPs) at small absolute gate voltages is, in our opinion, the consequence of the continuously distributed low density small sized Pt NPs with large Coulomb energy and defect induced trap sites outside the Pt NPs.[19–21] The strong influence of carriers' capture by trap sites outside of the Pt NPs on dynamical properties of write/erase processes under illumination of varying intensities and voltage pulse of different amplitudes and durations was discussed in Ref. 22, for nonvolatile memory devices based on similar structures. Due to different ΔE_g of small and large sized Pt NPs as well as energy depths of defect sites, the trapping processes are intensified at different gate voltage ranges. The result is the observed non-monotonic change of I_D with gate and drain voltages. It is evident that the magnitudes of applied voltages (vertical and lateral) in conjunction with illumination power can strongly influence the carriers' density variation in the channel region and hence dictate the NDR peaks or plateaus parameters, their form and location along the gate voltage scale. Specifically, the location of these peculiarities is marked by the arrows and illustrates their movement trajectory in Figures 2 and 3.

At large negative gate voltage increases the density of carriers (holes) induced in the silicon channel, and at the same time, it enhances the trapping probability by the Pt NP which causes a reduction in I_{DS}. For negative low V_G and under illumination, the minority carrier generation intensifies but the trapping efficiency is reduced and therefore a significant part of the carriers reaches the drain and I_D increases. A positive gate voltage shrinks the silicon depletion region under the gate dielectric so the minority carrier concentration is reduced and the photo generation process becomes rather insignificant making I_D almost constant. Finally, at large positive gate voltages, the current through the channel is due to accumulated majority carriers which can be trapped due to enhancement of the injection level so that I_D is reduced once more.

The maximum peak to valley current ratios (PVCR) in the dark and under illumination are, respectively, 60 (at $V_G = \pm 3$ V) and 140 or 26 (for $V_G = +3$ V and $V_G = -3$ V, respectively). In both regimes, the drain voltage was -3 V. These values are several times larger than those observed in Si-based field-induced band-to-band tunneling effect transistor,[23] resonant inter band tunneling diode based on Si/SiGe hetero structure,[24] or single Si-based MOS FET driven in the bipolar junction mode[25] where typical PVCR values are 2, 2.2, and 5.5, respectively. The peak photocurrent is almost 80 times larger than the peak current in the dark.

The dependence of the photocurrent versus illumination intensity (measured at 365 nm and a gate voltage of 0.15 V) is shown in Fig. 5(a) for various drain voltage levels. The characteristics are nearly linear and can be fit to a power exponent of 0.85 and 0.96 for V_D of +1 V, +2 V, and 0 V, respectively. The photo response increases by more than an order of magnitude for a drain voltage increase between zero and 1 V before it saturates. Detection responsivities versus illumination intensity are shown in Fig. 5(b) for two gate voltages, -0.15 V and -3 V and for different positive source to drain voltage values. The responsivity under a low

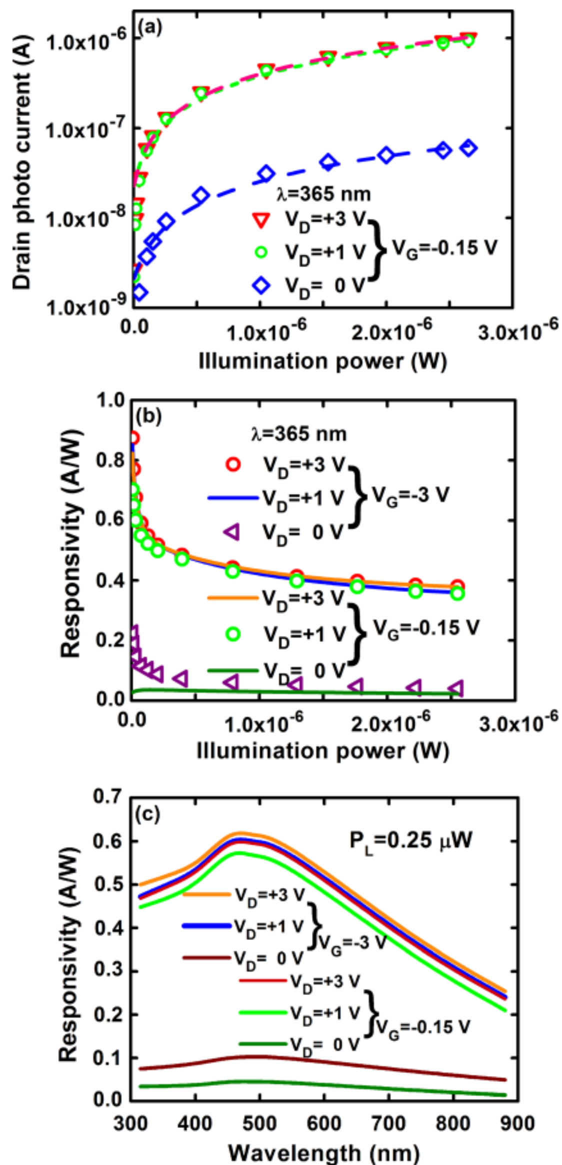

FIG. 5. Optoelectronic characteristics of structure with Pt NPs extracted from the I_D-V_G curves with various V_D and V_G values. (a) Photocurrent response versus illumination power. Dashed line is the linear fit result. (b) Responsivity versus illumination intensity at 365 nm. (c) Responsivity spectra.

illumination intensity of 0.25 μW and for $V_G = -0.3$ V and $V_D = +3$ V is very high, 0.53 A/W. It decreases with illumination intensity to 0.38 A/W at 2.5 μW. These responsivity values are significantly higher than those obtained for similar illumination intensities in back to back configured MIS diodes fabricated on SOI[2,3] or GaN based photodiodes.[26]

The spectral response of the three terminal device is shown in Fig. 5(c) for different V_G and V_D values. For $V_G = -3$ V and $V_D = +3$ V with an illumination intensity of 0.25 μW, the responsivity peaks at 455 nm where it reaches a value of 0.63 A/W. The interesting results are however at the spectral region edges. At 315 nm, the response reaches a record value of 0.50 A/W while at 880 nm it is 0. 26 A/W; both are more than 3 times larger than the previous results, measured for two terminal device.[2,3] The responses for a drain voltage of zero are much lower as shown in Fig. 5(c) for gate voltages of -0.15 V and -3 V and drain bias levels of $+1$ V, $+3$ V. The responsivity of structures with no Pt NPs is only half that of the structures with Pt NPs. This is qualitatively similar two terminal photodetectors fabricated in the same technology.[3]

The enhancement results from the vertical and lateral electric fields. A negatively biased gate electrode causes strong band banding in the silicon film. Under illumination, holes generated in the depletion region are swept towards the drain. The number of minority carriers, which reach the drain terminal depends strongly on the lateral electric field. Holes which are photo generated in the source region also contribute to the increase in responsivity. These holes transport to the depletion layer and enhance the density of the inversion layer. This in fact is demonstrated in Fig. 5(c) where an increase in the drain voltage from zero to $+3$ V and a rise of the absolute value of gate voltage from $|V_G| = 0$ to $|V_G| = 3$ V cause an increase in responsivity of almost one order of magnitude. This process differs from that, which occurs in two terminals of MIS or MSM type photodiodes.

To conclude, we have demonstrated a simple CMOS compatible three terminal devices that exhibits NDR with large peak to valley ratios and which also has a very large optical response, thereby can serve as an efficient photodetector as well as an important electronic component. Other devices which avail NDR include tunnel diodes which are two terminal devices and hence are inconvenient for some circuit integration.[6,27] Resonant tunneling systems are three terminal quantum devices but are fabricated from III–V materials and are not CMOS compatible. Moreover, the high optical sensitivity over a wide wavelength range offers additional functionalities, not possible in conventional NDR devices.

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