Manas Kumar Jena* and S. R. Samantaray

Synchrophasors-Assisted IPII-Based Intelligent Relaying for Transmission Lines Including UPFC

Abstract: This paper proposes a synchrophasors-assisted intelligent relaying scheme for transmission lines compensated by Unified Power Flow Controller (UPFC). The algorithm uses a new relaying signal termed as imaginary part of integrated impedance (IPII). The synchronized phasor measurements at both ends of the transmission line are used to extract voltage and current phasors from instantaneous voltage and current signals. The voltage and current phasors are utilized to derive IPII of each phase. Further, IPII of each phase is used as input to a data-mining model termed as decision tree (DT) which provides the final relaying decision. The proposed algorithm is validated on real-time digital simulator (RTDS) platform, and the results obtained indicate that the proposed scheme is both dependable and secure in protecting transmission system compensated by UPFC.

Keywords: imaginary part of integrated impedance (IPII), real-time digital simulator (RTDS), decision tree (DT), Unified Power Flow Controller (UPFC), transmission line relaying

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1 Introduction

Unified Power Flow Controller (UPFC) is one of the most versatile flexible AC transmission systems (FACTS) devices [1]. UPFC offers new horizons in terms of power system control with the potential to independently control three important power system parameters, for instance, bus voltage, line active power and line reactive power. Hence, UPFCs are used extensively for improving the utilization of the existing transmission system [1]. While the use of the UPFC improves the power transfer capability and stability of a power system, certain other problems emerge in the field of transmission system protection, affecting greatly the reach of the distance relay [2]. Depending on whether UPFC is present in the fault loop or not, the measured impedance at the relaying point would change [2]. When Static Synchronous Series Compensator (SSSC) of the UPFC consumes active power, the apparent resistance will increase and when SSSC consumes reactive power, the apparent reactance will increase [3]. Compared to Static Synchronous Compensator (STATCOM), UPFC has greater influence on the apparent resistance due to the active power injection and consumption by both SSSC and STATCOM. For a phase-to-phase fault, there is a tendency for the distance relay to under-reach and also for the earth element to mal-operate. Further, SSSC injects reactive power into the system; it behaves like a series capacitor and the apparent impedance decreases. On the other hand, when SSSC consumes reactive power it appears like series inductance and the apparent impedance increases [3]. Hence, depending upon the operating condition of UPFC during the fault, the distance relay may under-reach or over-reach.

In recent years many research work has been carried out in order to study the impact of FACTS devices like UPFC on the existing relaying schemes [3–6]. It is already established that the conventional distance relay is not reliable to protect transmission system compensated with UPFC. Hence, there is requirement of developing a new relaying algorithm for transmission system compensated with UPFC. There are basically two approaches to solve this problem. One of the approaches is to develop an adaptive trip boundarybased relaying scheme [6]. This approach is not reliable for real-time environment where tripping decision has to be taken reliably with minimum possible time lapse. The other approach is to develop a dedicated relaying algorithm for transmission system compensated with UPFC. This approach has gained its popularity mainly because the decision thresholds are not going to change in real time; rather these thresholds are set adaptively in the offline process.

Phasor measurement units (PMUs) using synchronization signals from the global positioning system (GPS) satellite system have evolved into mature tools and are

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now being utilized in the field of fault location [7]. In recent times, synchrophasor application to primary protection of transmission lines is gaining momentum mainly because of the advancement in the fibre opticsbased dedicated communication platform through which the three-phase voltage and current phasors can be transmitted from one end of the transmission line to the other reliably [6, 8–10]. Synchrophasors are increasingly contributing to the dependable and economical operation of power systems as real-time control and protection schemes become broadly used. In [6] a synchrophasors-assisted adaptive distance relaying approach has been suggested. The work suggests adaptive trip boundary-based distance relaying which is not quite reliable for real-time decision making. In [8] an adaptive fault locator technique is suggested for uncompensated transmission lines. Synchrophasorsassisted multiple features-based differential relaying scheme for transmission line including UPFC and wind farm is suggested in [9]. Synchrophasor application to UPFC compensated transmission lines is presented in [10].

Looking at the aforementioned protection challenges faced by the existing protection schemes, there is a strong motivation in developing a new intelligent relaying scheme for transmission lines compensated by UPFC. The research work has been carried out on real-time digital simulator (RTDS) platform, from RTDS Technologies, Winnipeg, Canada, RTDS uses parallel processing techniques (PB5 card) on rack-mounted processors to maintain continuous real-time digital simulation of a power system of arbitrary complexity. The proposed imaginary part of integrated impedance (IPII)-based intelligent relaying is based on pre-processing the instantaneous current and voltage time domain signals using the GTNET-PMU card (Giga-Transceiver Network Communication Phasor Measurement Unit Card) [11]. The PMU algorithm used in this component is the P class reference algorithm from Annex C of the IEEE C37.11.8.1–2011 standard [12]. The GTNET-PMU component output is synchronized to an external 1PPS signal via the GTSYNC card. Thus, synchronized voltage and current phasors are computed at both ends of the line containing UPFC, from which IPII for each phase is calculated. Once the IPIIs are computed, a data-mining model known as decision tree (DT) [13–15] is developed using the magnitude of IPII set. The developed DT is used to take the final relaying decision. This paper is organized as follows: Section 2 describes the principle of IPII-based protection, Section 3 explains the system under study and Section 4 shows the results obtained from the simulation studies. Section 5 concludes the manuscript.

2 Concept of IPII

The proposed relaying scheme is developed using a new signal termed as "IPII". Initially, the concept of IPII is explained for a single-circuit transmission line. The following parameters are considered for deriving IPII:

 $E_{\rm s}$, $E_{\rm r}$: Voltages of sources at sending end and receiving end of the transmission line, respectively.

 \overline{V}_{s} , \overline{V}_{r} , \overline{I}_{s} , \overline{I}_{r} : Voltage and current phasors measured at the sending end bus and receiving end bus, respectively.

 \overline{V}_{se} : Series injection voltage of UPFC

 \overline{I}_{sg} , \overline{I}_{rg} : Currents through the equivalent capacitance at sending end(s) and receiving end(r), respectively

 \overline{I}_{f} : Current through the fault branch with fault resistance of R_{f} .

 \bar{I}_{sh} : Shunt current injected or absorbed by Shunt converter of UPFC

 $Z_{\rm s}$, $Z_{\rm r}$: Equivalent impedance of power source at sending end and receiving end

 $Z_{\rm sg}(=2/Y)$, $Z_{\rm rg}(=2/Y)$: equivalent lumped capacitive impedances of the line.

 Z_{ls} : Line impedance from sending end to the point F Z_{lr} : Line impedance from receiving end to the fault point F

 Z_l : Entire line impedance

 $Z_{\rm se}$: Impedance offered by series converter of UPFC Transmission line: π -equivalent circuit Mathematically IPII is defined as follows:

$$IPII = imag(II) \tag{1}$$

where
$$II = \left(\frac{\Delta \overline{V}}{\Delta \overline{I}}\right) = \left(\frac{\overline{V}_{s} + \overline{V}_{r}}{\overline{I}_{s} + \overline{I}_{r}}\right)$$
 (2)

$$IPII = imag\left(\frac{\overline{V}_{s} + \overline{V}_{r}}{\overline{I}_{s} + \overline{I}_{r}}\right)$$
(3)

2.1 Characteristics of IPII for external faults in case of transmission lines compensated by UPFC

The equivalent circuit of the system with the transmission line compensated with UPFC is shown in Figure 1.

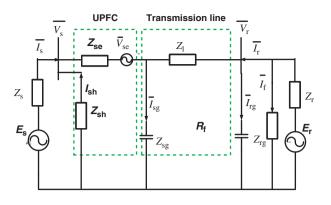


Figure 1: Equivalent circuit of the UPFC-compensated transmission system for an external fault.

Now, the integrated current can be obtained as

$$egin{aligned} \Delta ar{I} &= ar{I}_{ ext{s}} + ar{I}_{ ext{r}} = ar{I}_{ ext{sg}} + ar{I}_{ ext{rg}} \pm ar{I}_{ ext{sh}} \ &= rac{[\overline{V}_s - ar{I}_{ ext{se}} Z_{ ext{se}} + \overline{V}_{ ext{se}}]}{Z_{ ext{sg}}} + rac{[\overline{V}_r]}{Z_{ ext{rg}}} \pm ar{I}_{ ext{sh}} \end{aligned}$$

 $\bar{I}_{sh} = +V_e$ if shunt converter injects reactive current into the Bus

 $\bar{I}_{sh} = -V_e$ if shunt converter absorbs reactive current from the Bus

$$\Rightarrow \mathrm{II} = \left(\frac{\Delta \overline{V}}{\Delta \overline{I}}\right) = \left(\frac{\overline{V}_{\mathrm{s}} + \overline{V}_{\mathrm{r}}}{\left[\frac{\overline{V}_{\mathrm{s}} - \overline{I}_{\mathrm{se}} Z_{\mathrm{se}} + \overline{V}_{\mathrm{se}}\right]}{Z_{\mathrm{sg}}} + \frac{\overline{V}_{\mathrm{r}}}{Z_{\mathrm{rg}}} \pm \overline{I}_{\mathrm{sh}}\right)$$
(4)

 \overline{V}_{se} and the value of voltage drop $\overline{I}_{se}Z_{se}$ are relatively small. So the above equation can be approximated as

IPII
$$\approx 2/Y$$

 \Rightarrow IPII = imag(II)[Higher absolute value with negative sign]

It is observed that when external fault occurs, the IPII represents capacitive reactance of the line whose value is negative with a higher magnitude, because of the line capacitive current.

2.2 Characteristics of IPII for internal faults in case of transmission lines compensated by UPFC

Figure 2 shows the equivalent circuit of the system with the transmission line compensated by UPFC with an internal fault. Let the ratio of distance from the fault point to the sending end to that of the entire line is *m*. Thus, $Z_{ls} = mZ_{l}, Z_{lr} = (1 - m)Z_{l}$:

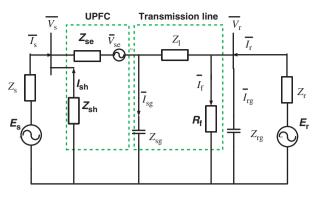


Figure 2: Equivalent circuit of the UPFC compensated transmission system for an internal fault.

$$Z_1 = Z_s + Z_{ls} + Z_{se} = Z_s + mZ_l + Z_s$$
$$Z_2 = Z_r + Z_{lr} = Z_r + (1 - m)Z_l$$

When the capacitances of the line is ignored, the current through the fault branch is

$$\overline{I}_{\rm f} = \overline{V}_{\rm f} / (R_{\rm f} + Z_1 \parallel Z_2) \tag{5}$$

Where \overline{V}_f is the voltage at the fault point before the fault occurred, which can be expressed as follows:

$$\begin{split} \overline{V}_{\rm f} &= k(\overline{V}_{\rm s} + \overline{V}_{\rm r}) {\rm e}^{j\delta}, \\ \Delta \overline{I} &= \overline{I}_{\rm s} + \overline{I}_{\rm r} \pm \overline{I}_{\rm sh} = \overline{I}_{\rm sg} + \overline{I}_{\rm rg} + \overline{I}_{\rm f} \pm \overline{I}_{\rm sh} \\ &= \frac{(\overline{V}_{\rm s} - \overline{I}_{\rm se} Z_{\rm se} + \overline{V}_{\rm se})}{Z_{\rm sg}} + \frac{(\overline{V}_{\rm r})}{Z_{\rm rg}} \\ &+ [k(\overline{V}_{\rm s} + \overline{V}_{\rm r}) {\rm e}^{j\delta} / (R_{\rm f} + Z_1 ||Z_2)] \pm \overline{I}_{\rm sh} \\ &\approx \frac{(\overline{V}_{\rm s} + \overline{V}_{\rm r})}{2/Y} + [k(\overline{V}_{\rm s} + \overline{V}_{\rm r}) {\rm e}^{j\delta} / (R_{\rm f} + Z_1 ||Z_2)] \pm \overline{I}_{\rm sh} \end{split}$$
(6)

Now,

$$IPII \approx imag\left(1/\left(\frac{1}{2/Y} + \frac{ke^{j\delta}}{(R_{\rm f} + Z_1||Z_2)}\right)\right)$$

$$\approx imag[2/Y||((R_{\rm f} + Z_1||Z_2)/(ke^{j\delta}))]$$
(7)

It is observed from (7) that IPII is a function of fault location, fault resistance, power angle δ , source impedance and line impedance. In no-fault conditions (or in external fault condition), the sign of the IPII (which reflects the impedance of the line capacitance) is negative with large absolute value. However, in case of internal faults, the sign of the IPII is either positive or negative with smaller magnitude. Thus, based on the magnitude of IPII, the external and internal faults can be distinguished. However, after extensive simulations of the tested power system, it is observed that the magnitude of IPII changes following changes in fault parameters like fault

resistance, fault location, UPFC modes of operation, etc. Thus, it is necessary to have an intelligent threshold setting of IPII. This is achieved in the offline process using a data-mining model known as DT. Once the trained DT is obtained, the same is used in the online process for testing purpose. DT is constructed using a set of training samples and is then applied to classify a set of unseen samples that are called test samples. DT is constructed using a top-down search performance for data classification. It starts from a root node and samples are then classified by posing a series of questions about the features associated with the data. A node is divided into two sub branches according to the possible answers for its question. In Rattle [16], a DT has a binary structure with two types of nodes, the internal node with two child nodes and terminal node without any child node. Each terminal node provides a prediction result of the form secure (S), insecure (I) or a performance index value. For the purpose of training a good DT, a learning set and a test set in the same format are required. The learning set is first used to train a maximal tree by recursively splitting a parent node into two purer child nodes until further splitting can no longer improve accuracy and this maximal tree is then pruned step by step to generate a series of smaller DTs in order to attenuate the overfitting problem. The main goal is to partition all the cases in a high-dimensional space into various subregions with homogeneous cases in each region. Details regarding splitting and stopping rules and DT pruning algorithms are provided in [16].

In the proposed scheme, IPII of all the three phases are used as input to the DT. The target outputs (classes) are categorized as 0(Normal or external Fault), 1(a-g Fault), 2 (b-g Fault), 3(c-g Fault), 4(a-b/a-b-g Fault), 5(b-c/b-c-g Fault), 6(c-a/c-a-g Fault), 7(a-b-c Fault). That means the final relaying decision will show either no fault condition or will give the faulted phase(s) if there is any internal fault occurring within the zone of protection. The Rattle [16] software package is used to build the DT for final relaying decision. The DT is trained in the offline process using RATTLE software package. Once the optimal DT is found, the same is further used for testing propose in the online process in real time. The proposed study considers wide variation in operating and fault conditions to generate data set, and the variations are as follows.

- Variation in fault resistance $(R_{\rm F})$ from 0 to 300 Ω
- Variation in fault location: 20%, 30%, 50%, 70%, 80% and 95% of the total line length
- Variation in fault inception angle (FIA): 0°, 30°, 60°, 90°
- Different types of fault: a-g, b-g, c-g, a-b, b-c, c-a, ab-g, bc-g, ca-g, a-b-c

 UPFC mode of operations: automatic power flow control mode (APFC) and bypass mode

The complete data set generated considering above variations are used to train and test the DT. The flowchart of the proposed scheme is illustrated in Figure 3. PMUs are used to extract voltage and current phasors at both ends of the transmission line which are used to calculate IPII of each phase of the transmission line. The IPIIs are used as input to train the DT. Thus, the trained DT is obtained using the RATTLE software package (offline process). The trained DT is used further for testing purpose (online process) on RTDS platform.

The proposed scheme needs a robust and reliable communication platform. Modern-day high-speed communication networks typically use synchronized optical network (SONET) or synchronized digital hierarchies (SDH) standard for communication with transmission rates of the order of 274.2 Mbps or 155.5 Mb/s, respectively. They permit "network protection" that is, during failure of a communication link, communication services are restored by reconfiguring flow of information in alternate paths. A typical example is self-healing ring architecture used with SONET [17, 18]. In such networks, synchronization by delay equalizers becomes difficult due to channel asymmetry. Due to channel asymmetry, communication delays for transmission and reception paths are not identical. Thus, the current samples are time stamped by a GPS which enables retrieving signals with same time stamp and, thus providing immunity to channel delays, asymmetry, etc. Further, dynamic estimate of the channel delay can be easily maintained by subtracting the GPS time stamp at the sending end from the receiving end time stamp. This permits back up operation even during GPS failure modes. The proposed scheme can reliably work on the communication platform as devised in [17, 18].

3 Fault simulation and building DT

A 500 kV, 60 Hz transmission system including UPFC is illustrated in Figure 4. This system constitutes of two substations and one UPFC is located at one end of the 400 km transmission line (distributed model). The transmission line has the following parameters:

 $R_1 = 0.01537$ (Ω /km): Positive sequence resistance $R_0 = 0.04612$ (Ω /km): Zero sequence resistance $L_1 = 0.8858 \times 10^{-3}$ (H/km): Positive sequence inductance $L_0 = 2.654 \times 10^{-3}$ (H/km): Zero sequence inductance $C_1 = 13.06 \times 10^{-9}$ (F/km): Positive sequence capacitance $C_0 = 4.355 \times 10^{-9}$ (F/km): Zero sequence capacitance

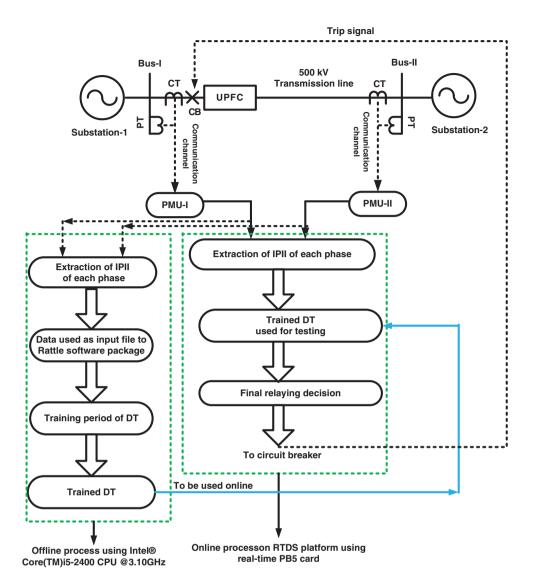


Figure 3: Flowchart of the proposed scheme.

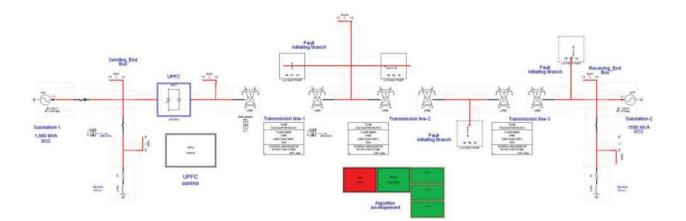


Figure 4: Single line diagram representation of the transmission system developed on RTDS for testing the proposed relaying scheme.

The details of the UPFC model used in the proposed scheme are derived from [19]. The fault simulations on RTDS platform are carried out with various operating conditions. Total fault cases simulated for the system are 10 ($R_{\rm F}$) × 4(FIA) × 10 (types of fault) × 5 (fault locations) \times 3 (V_{se} – UPFC voltage) = 6,000. The DT is trained and tested for different combination of data set such as (20-80), (30-70), (40-60), (70-30) for training and testing purpose, respectively. For example in combination of (70-30) data set, 70% of total data set are considered for training purpose and rest 30% for testing purpose. Figure 5 shows the trained DT with 70% training data set and tested on rest unseen 30% data set. The confusion matrix with (70-30) date set generated for the above system is shown in Table 1, which provides the performance accuracy of predicted cases against actual cases. DT provides confusion matrix only on testing data set [20]. For example, (70-30)% data set mean, the confusion matrix provides classification results on 30% of total data set. Here total 1,800(60-Normal case/external fault, 460ag fault, 400-bg fault, 378-cg fault, 100-ab fault, 132-bc fault, 130-ca fault, 140-abc fault) fault cases were taken for testing purpose.

It is observed from the confusion matrix that the trained DT provides 100% classification accuracy against each fault cases.

Simulation results for remote end faults (fault location = 85% of line, $R_{\rm F} = 100 \ \Omega$, FIA = 0°) are shown in Figures 6–8. Figure 6(a) shows the magnitude of IPII for a-g fault at remote end of the line and it is observed from that IPII magnitude of the faulted phase goes to the positive value, while other unfaulted phase remains marginally affected.

Figure 6(b) shows that the trained DT provides trip signal only for the faulted phase making the proposed scheme selective in selecting faulted phase(s) involved in the fault process. It is also observed from Figure 6(b) that the fault inception occurs at 0.04 s and trip signal from DT comes at 0.05 s. Hence, the response time of the proposed scheme is 10 ms excluding the communication delay time. The inclusion of communication delay will not affect the performance indices such as dependability and security of the relay. However, the response time of the relay will be further delayed by the communication delay time (order of 4 ms [17]). Similar observations are made for a-c fault. Figure 7(a) shows that following

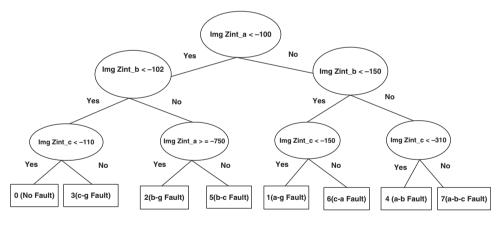


Figure 5: Decision tree generated after training period for the studied UPFC compensated transmission system.

Predicted actual	0 (No-fault)	1 (a-g)	2 (b-g)	3 (c-g)	4 (a-b/a-b-g)	5 (b-c/b-c-g)	6 (c-a/c-a-g)	7 (a-b-c)
0(Normal)	60	0	0	0	0	0	0	0
1(a-g)	0	460	0	0	0	0	0	0
2(b-g)	0	0	400	0	0	0	0	0
3(c-g)	0	0	0	378	0	0	0	0
4(a-b/a-b-g)	0	0	0	0	100	0	0	0
5(b-c/b-c-g)	0	0	0	0	0	132	0	0
6(c-a/c-a-g)	0	0	0	0	0	0	130	0
7(a-b-c)	0	0	0	0	0	0	0	140

Table 1: Confusion matrix generated during testing of proposed scheme for UPFC-based system.

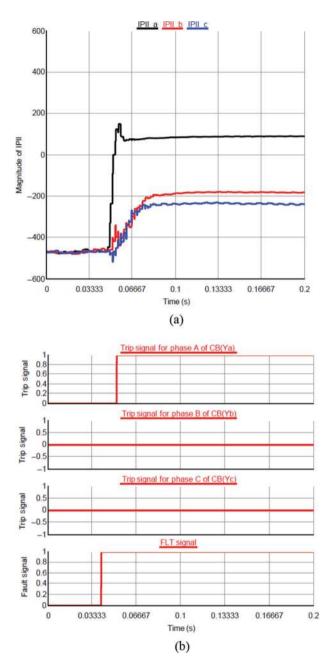


Figure 6: (a) IPII magnitude of different phases during remote end internal a-g fault. (b) Trip signals of different phases during remote end internal a-g fault.

occurrence of a-c fault IPII of phase-a and phase-c moves from -480 to +80 indicating the faulted phases involved in the fault process, whereas IPII of phase-b remains marginally affected. Figure 7(b) shows DT output for circuit breakers (CB), which shows that the trained DT provides trip signal only for the faulted phase(s). Figure 8 (a) shows that following occurrence of a-b-c fault, IPII of phase-a, phase-b and phase-c moves from -480 to +100indicating that all the three phases are involved in the

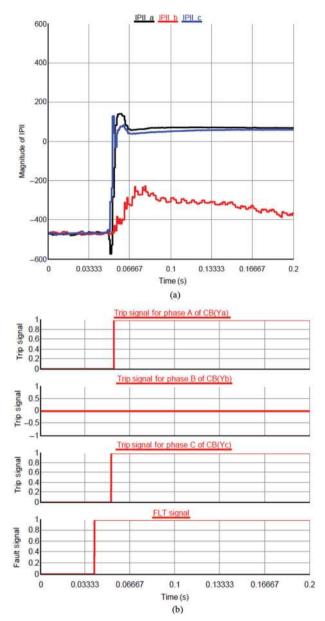


Figure 7: (a) IPII magnitude of different phases during remote end internal a-c fault. (b) Trip signals of different phases during remote end internal a-c fault.

fault process. Figure 8(b) shows DT output for CB, which shows that the trained DT provides trip signal for all the faulted phases.

4 Performance assessment and discussion

The previous section deals with the design and development of IPII-based relaying scheme for UPFC-compensated

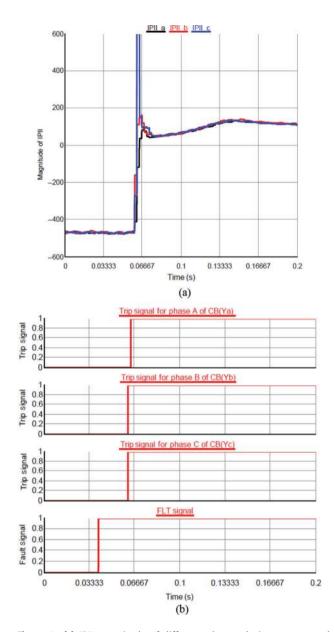


Figure 8: (a) IPII magnitude of different phases during remote end internal a-b-c fault. (b) Trip signals of different phases during remote end internal a-b-c fault..

transmission system. To assess the performance of the proposed intelligent relaying scheme, two statistical metrics are defined as follows:

(i) **Dependability**: Dependability is defined as the measure of the certainty that the relays will operate correctly for all the faults for which they are designed to operate [15].

Dependability (*D*) = Total number of fault cases predicted/Total number of actual fault cases.

 (ii) Security: Security is defined as the measure of the certainty that the relays will not operate incorrectly (maloperate) for any other power system disturbance.

Security (S) = Total number of external faults predicted as external fault/Total number of external faults [14].

4.1 Comparison with distance relaying

The performance of the proposed scheme is compared with conventional distance relaying (Mho relay). Different fault cases (100 cases) are simulated with different fault locations (with $R_{\rm F} = 1 \Omega$, FIA = 0°). In all the 100 test cases, only the shunt voltage source inverter is connected to the UPFC system and it operates as STATCOM alone. It is observed that the proposed scheme is 100% dependable (Table 2) for remote end faults where the distance relaying fails measurably giving in between 22% and 25% for the same index. The reason behind this kind of result is that in the STATCOM mode of operation of UPFC, the distance relay mostly under-reaches as already verified in [3]. Hence, even if the zone-I coverage of the distance relay is set to 85% of the line, the actual relay coverage is always less than 85% which results in such low accuracy level. Because the proposed scheme is a unit protection scheme and uses signals from both ends

 Table 2: Dependability comparison between distance relaying and proposed relaying scheme for different fault locations.

Scheme	D (%) (fault at 10% of line)			D(%) (fault at 85% of line)		
	LG	LL	LLL	LG	ш	LLL
Distance relaying	100	100	100	20	22	25
Proposed intelligent relaying	100	100	100	100	100	100

of the transmission line for final decision making. Hence, fault location is not going to affect any of the performance indices of the proposed intelligent relaying scheme.

4.2 Effect of High fault impedance on the proposed scheme

Faults involving high fault impedance pose a problem to conventional relaying schemes. In order to check the performance of the proposed relaying scheme for faults with higher fault impedance different cases are tested and the results are depicted in Table 3. It is observed that even though IPII value of the faulted phase decreases with increase in fault resistance, the trained DT could able to give correct relaying decision. This is because of the intelligent threshold of the trained DT.

4.3 Effect of level and mode of compensation

UPFC does not always transit to bypass mode for all the variations in fault parameters. In order to study the effect of UPFC modes of operation upon the proposed relaying scheme, total 80 fault cases (variations of R_F from $R_F = 1$ to 300 Ω , FIA = 0°) with different level of compensation

and modes of operation are tested and it is found that the dependability of the proposed scheme is independent of the above variations as depicted in Table 4.

4.4 Security of the proposed scheme

Any relaying scheme should be able to distinguish external faults from internal faults. This attribute of any relaying algorithm is commonly called as "security" of the scheme. Security of the proposed scheme is already tested in Section 3 (Table 1). Sixty numbers of external fault cases are given as test input to the trained DT and it is observed from Table 1 that the number of predicted output is same as the actual number of inputs. That means all 60 external fault cases are classified as external faults.

4.5 Comparison with current differential protection

The well-known current differential protection criterion must set a current threshold higher than the steady capacitive current of the line to avoid maloperation [21]. During normal operating condition, the capacitive current of the studied system is about 500 Å. The differential

 Table 3: Performance of the proposed scheme for faults with high impedance.

Fault type	IPII-a phase	IPII-b phase	IPII-c phase	DT output
a-g, $R_{ m F}=1~\Omega$	100	-500	-500	1
a-g, $R_{\rm F}=150~\Omega$	10	-500	-500	1
a-g, $R_{\rm F}=250~\Omega$	-5	-500	-500	1
a-b, $R_{\rm F}=1~\Omega$	100	100	-500	4
a-b, $R_{\rm F}=$ 150 Ω	15	15	-500	4
a-b, $R_{\rm F}=$ 250 Ω	-6	-6	-500	4
a-b-c, $R_{\rm F} = 1~\Omega$	100	100	100	7
a-b-c, $R_{\rm F}=150~\Omega$	12	12	12	7
a-b-c, $R_{\rm F}=250~\Omega$	-7	-7	-7	7

Table 4: Effect of UPFC mode and compensation level on dependability of the proposed relaying scheme.

Types of fault				Dependability (%)
	Bypass mode (20 cases)	APFC mode (20 cases)	Bypass mode (20 cases)	APFC mode (20 cases)
a-g	100	100	100	100
a-b	100	100	100	100
a-b-g	100	100	100	100
a-b-g a-b-c-g	100	100	100	100

current setting of the current differential protection should be set above two times the operating capacitive current in order to avoid maloperation. Thus, for the studied system the differential current setting should be set as 1,000Å. It is observed that the differential current of faulty phase is below 1,000 Å when the fault resistance exceeds 100 Ω . Total 90 fault cases are taken as test cases (10 cases from each fault type) with variations in fault resistance and other fault parameters. It is found that for faults with more than 100 Ω fault resistance, dependability of the current differential scheme reduces, whereas the dependability of the proposed scheme remains at 100% for all fault resistance as depicted in Table 5.

Table 5: Dependability comparison between current differential scheme and proposed relaying scheme for different fault resistances.

Fault type	D(%)		
	Current differential	Proposed scheme	
a-g, $R_{\rm F}$ =1 Ω	100	100	
a-g, $R_{\rm F}$ =100 Ω	80	100	
a-g, $R_{\rm F}=$ 200 Ω	50	100	
a-b, $R_{\rm F}$ =1 Ω	100	100	
a-b, $R_{\rm F}$ =100 Ω	80	100	
a-b, $R_{\rm F}=$ 200 Ω	60	100	
a-b-c, $R_{\rm F}=1~\Omega$	100	100	
a-b-c, $R_{\rm F}$ =100 Ω	80	100	
a-b-c, $R_{\rm F}=$ 200 Ω	60	100	

4.6 Implementation of the proposed scheme

The intelligent relay module can be programmed on a digital signal processing (DSP)/field-programmable gate array (FPGA) board. In this case it is the DT (Figure 5) that has to be programmed on a DSP/FPGA board. For example, looking at Figure 5, in order to classify an a-g fault the condition to be coded on a DSP board is "if Img Zint_a > -100 and Img Zint_b < -150 and Img Zint_c < -150", then there is an a-g fault on the transmission line. The only difference is that instead of positive sequence impedance (existing distance relay), IPII (proposed scheme) is used as the relaying signal in the proposed scheme.

5 Conclusions

The paper presents IPII-based intelligent relaying scheme for UPFC-compensated transmission lines. The process starts at pre-processing the voltage and current signals using GTNET-PMU which supports C37.118.1-2011 IEEE standard, and the derived integrated impedances are used to build the optimal DT in selecting the faulty phase(s) involved in the fault process. The scheme is both dependable and secure in protecting UPFC-compensated transmission system. The scheme is validated on RTDS platform. The response time of 10 ms from the fault inception on RTDS platform shows the fastness of the proposed relaying scheme.

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