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A Constrained Inter-Submodule State-of-Charge Balancing Method for Battery Energy Storage Systems Based on the Cascaded H-Bridge Converter

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***Abstract*—In the operation of battery energy storage systems (BESSs) based on the cascaded H-bridge (CHB) converters, it is desirable to balance the state of charge (SoC) among the submodules (SMs) within each phase arm. However, there are constraints on the active power distribution among the SMs that intends to balance the SoC. For instance, each SM in a practical system is designed with a specific power rating and can be damaged if it is exceeded. Therefore, a novel rule-based method is proposed in this paper to achieve a fast SoC balancing while respecting the power constraints of the SMs. The proposed method is general and readily applicable to hybrid BESSs, where the SMs are integrated with heterogeneous energy storage. Experimental results are obtained to verify the effectiveness of the proposed algorithm and to compare its performance with respect to existing methods.**

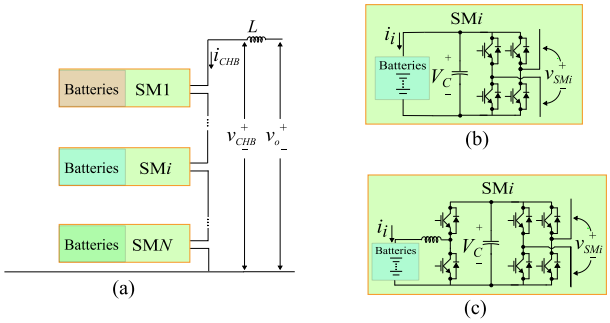

Fig. 1. Circuit diagram of (a) CHB converter-based BESS, (b) battery modules directly connected to the SM, and (c) battery modules connected to the SM via a boost converter.

I. Introduction

The share of renewable energy sources in global electricity generation has increased to 29% by 2020, where the solar photovoltaic (PV) and wind contribute two-thirds of the growth [1]. Consequently, battery energy storage systems (BESSs) are required in the power system to compensate for the intermittency and fluctuations in the generated renewable power [2]. The cascaded H-bridge (CHB) converter is a suitable candidate to integrate the BESS into the power system, especially in medium-/high-voltage applications [3]–[6]. Compared to the conventional two-level converters, advantages of the CHB converter include modularity, better harmonic performance, lower switching frequency, ability to accommodate heterogeneous energy storage, etc. [7]–[9].

Fig. 1(a) depicts the circuit diagram of a single-phase CHB converter-based BESS, which consists of N submodules (SMs). Battery modules are integrated into the SMs directly or via a dc-dc converter, as depicted in Figs. 1(b) and (c) [10], respectively. Ideally, the battery modules of all the SMs are identical and operate symmetrically in a BESS, which is referred to as symmetric BESS in this paper. There is also nowadays interest in hybrid BESSs, which consists of different battery modules and operates asymmetrically [11]. As an example, it is economic to use second-life batteries of electric vehicles, with different state of health (SoH), power rating and capacity, etc. [12]. Another example is employing a proper combination of high-energy batteries and high-power batteries to effectively reduce the required number of batteries and cost of a BESS [13].

Despite the aforementioned benefits, hybrid BESSs present challenges while balancing the state of charge (SoC) among the SMs within the phase arm. SoC balance is important as it enables a BESS to fully utilize its power and energy capacities [14]. For instance, without proper SoC balancing, the batteries in some SMs may be fully discharged much faster than the batteries in other SMs, leading to a reduced active power capacity.

The conventional inter-SM SoC balancing methods for the CHB-based BESS can be classified into two main categories, viz., those based on proportional and integral (PI) controllers [15]–[17], and those using a sorting stage [18]–[20].

The PI-based methods [15]–[17] modify the output voltage references of the SMs by adding a fundamental-frequency voltage component, which is in phase with the arm current and whose amplitude is calculated with a PI controller according to the SoC unbalance among the SMs. The modification of SM output voltage references leads to different SM active powers, which balance the inter-SM SoCs. However, as the SM active power is implicitly modified by the PI controller, this category of methods lacks an explicit mechanism to constrain the active powers within safe operating ranges. Moreover, the design of the control gains in the PI controller is affected by the battery capacities of each SM [16], which makes it challenging to design the PI parameters when applied to hybrid BESSs as the battery capacities can vary among the SMs.

The sorting-based methods [18]–[20] first decide the number of SMs to insert and their polarity (either positive or negative) at each sampling period. Then, based on the SoC values of the SMs and the arm current direction, a sorting stage is used to choose which SMs to insert, which affects the SM active powers and hence balances the SoC. Similar

to the PI-based methods, sorting-based methods also lack an explicit mechanism to constrain the SM active powers within safe operating ranges as the powers are implicitly modified by the sorting stage. Moreover, even with a mild SoC unbalance among the SMs, the sorting stage can significantly modify the SM active powers, hence some SMs will be charged/discharged with relatively large powers that can shorten the lifespan of batteries.

From the above discussion, there is a dearth of the inter-SM SoC balancing methods that can effectively balance the SoC, while constraining the active powers of the SMs within a safe range. To address this gap, this paper firstly investigates the performance of the existing SoC balancing methods and reveals their drawbacks. Afterward, the paper proposes a rule-based SoC balancing algorithm that overcomes the drawbacks of the existing methods without compromising the SoC balancing capability. The proposed algorithm is applicable to symmetric and hybrid BESSs, which makes it general.

The rest of this paper is organized as follows. Section II examines the existing SoC balancing methods and reveals their drawbacks. Section III introduces the proposed rule-based method. Experimental results are provided in Section IV. Finally, Section V summarizes the main conclusions of the paper.

II. Conventional SoC Balancing Methods

This section firstly introduces the principle of the SoC balancing. Afterward, the existing SoC balancing methods are reviewed.

A. SoC Balance

In a CHB converter-based BESS with N SMs per phase, which is depicted in Fig. 1 (a), the SoC of the battery module in the ith ($i \in [1, N]$) SM is calculated using the Coulomb Method [21]:

$$SoC_i(t) = SoC_i(0) + \frac{\int_0^t i_i dt}{Q_i}, \tag{1}$$

where $SoC_i(t)$ and $SoC_i(0)$ correspond to the instantaneous SoC and the initial SoC, respectively, i_i refers to the battery current, and Q_i denotes the capacity of the battery module. Note that SoC_i is within the range [0%, 100%]. Although i_i may contain considerable low- and high-frequency ripple, SoC_i can be considered free of the ripple as Q_i is usually large for batteries. The capacity Q_i corresponds to [22]:

$$Q_i = Q_{nom\text{-}i} \times SoH_i, \tag{2}$$

where $Q_{nom\text{-}i}$ and SoH_i refer to the nominal capacity and SoH of the battery module in the ith SM, respectively.

The average value of i_i in a fundamental period corresponds to:

$$\bar{i_i} = \frac{\bar{P}_{bi}}{V_{bi}}, \tag{3}$$

where $\bar{P}_{bi}$ and V_{bi} are the average active power and voltage of the battery module in the ith SM, respectively. The value of

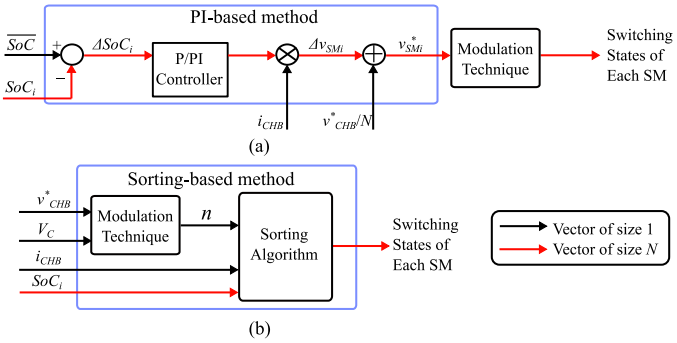

Fig. 2. Conventional SoC balancing methods: (a) PI-based method, and (b) sorting-based method.

$\bar{P}_{bi}$ depends on the average active power of the corresponding SM:

$$\bar{P}_{bi} = \eta_i \bar{P}_i, \tag{4}$$

where $\bar{P}_i$ refers to the average active power of the SM and η_i denotes the ratio of $\bar{P}_{bi}$ to $\bar{P}_i$. When $\bar{P}_i > 0$, which means the SM is charging, η_i is below one due to the power converter loss in the SM. When $\bar{P}_i < 0$, which means the SM is discharging, η_i may be one or higher than one [14]. The value of $\bar{P}_i$ corresponds to

$$\bar{P}_i = \frac{1}{T}\int_{t_0}^{t_0+T} v_{SMi} i_{CHB} dt, \tag{5}$$

where T refers to the fundamental voltage period, v_{SMi} refers to the output voltage of the ith SM, and i_{CHB} refers to the arm current of the CHB converter. Note that v_{SMi} is within $[-V_C, V_C]$, where V_C refers to the capacitor voltage. Moreover, v_{SMi} can differ among the SMs, thus providing a degree of freedom to modify the active power of each SM. In fact, the existing SoC balancing methods [15]–[19] modify the output voltage of the SMs based on their SoC values, leading to different battery currents, and hence different active powers, that aim at balancing the SoC values.

B. PI-Based Methods

PI-based methods [15]–[17] modify the output voltage references of the SMs by adding a fundamental-frequency voltage component, denoted as Δv_{SMi}, which is in phase with the arm current i_{CHB}. The amplitude of Δv_{SMi} is calculated by a PI controller according to the SM SoC unbalance.

As an example, Fig. 2(a) depicts the SoC balancing method in [16]. Denoting the mean SoC as $\overline{SoC}$ ($\overline{SoC} = \frac{1}{N}\sum_{i=1}^{N} SoC_i$), the SoC unbalance of the ith SM corresponds to:

$$\Delta SoC_i = \overline{SoC} - SoC_i. \tag{6}$$

The voltage component Δv_{SMi} is then calculated as

$$\Delta v_{SMi} = K_p \Delta SoC_i i_{CHB}, \tag{7}$$

where K_p is the control gain. Thus, the product of Δv_{SMi} and i_{CHB} generates an active power proportional to ΔSoC_i that balances the SoC. Note that $\sum_{i=1}^{N} \Delta v_{SMi} = 0$ and hence, the total active power of the BESS is unaffected.

Although the results in [15]–[17] show that PI-based methods can balance the inter-SM SoC when applied to symmetric BESSs, they have some drawbacks:

(i) The output voltage of each SM is limited to a fundamental-frequency component only, which weakens the SoC balancing capability. According to [23], by adding components of other frequencies to the fundamental-frequency voltage, the SMs can process more active power. Accordingly, this paper uses this ability to enhance SoC balancing capability.

(ii) It is difficult to limit the active power of each SM within a prescribed safe range since the active powers are indirectly affected by the output of the PI controller. The calculation of Δv_{SMi} does not consider its effect on the SM active power. Moreover, if a saturation stage is added to the output of the PI controller, the sum of SM output voltages can be different from the reference voltage of the converter, which affects the total active power of the BESS.

(iii) It is not trivial to design the PI parameters when applied to hybrid BESSs because the SoC balancing time constant is related to the battery capacities [16].

C. Sorting-Based Methods

Sorting-based methods [18], [19] use a sorting stage to decide the operation mode of each SM at each sampling step, according to their corresponding SoC and the arm current direction.

As an example, Fig. 2(b) depicts the SoC balancing method in [18]. According to the converter voltage reference v^*_{CHB} and the SM capacitor voltages V_C, the required number of SMs to insert is derived, and denoted as n ($n \in [1, N]$). Based on i_{CHB}, n, and the SoC of each SM, a sorting method is used to select the SMs to insert with a similar polarity to v^*_{CHB}. When v^*_{CHB} and i_{CHB} have similar polarities, which means the inserted SMs will be charged, the n SMs with the lowest SoC will be inserted while the others will be bypassed. Otherwise, the n SMs with the highest SoC will be inserted while the others will be bypassed.

Similar to the PI-based methods, the sorting-based methods cannot constrain the active power of each SM since the SM active power is not considered in the sorting stage. Moreover, with sorting-based methods, the SM output voltages normally have the same polarity as the converter voltage, which can weaken the active power capability of the SMs [23].

To conclude, the existing methods have important drawbacks that limit their application. To overcome the aforementioned drawbacks, a novel rule-based SoC balancing method is developed in the next section.

III. Proposed Rule-Based Method

The conventional inter-SM SoC balancing methods directly modify the SM output voltages v_{SMi} according to the SoC unbalances, which indirectly decide the active power distribution among the SMs. Consequently, the SM active powers can become unsafe. For example, charging a SM with a higher power than its rated value will damage the integrated batteries and switches. To overcome this challenge, the proposed method explicitly calculates the active power reference of each SM that balances their SoC values, with consideration of constraints in SM active powers. Moreover, the differences in the integrated battery modules (SoH, power rating, etc.) are considered in the calculation of the power references, which makes the proposed method general and suitable for hybrid BESSs.

A. SM Active Power Constraints

In the operation of a BESS based on the CHB converter, the constraints in the SM active powers can be classified into three different categories, which are referred in this paper as hardware constraints, summation constraints, and disparity constraints.

1) Hardware Constraints: In practice, the maximum power that a SM can process is limited by its components, such as the integrated battery modules, the power switches, etc. The hardware constraints can be formulated as inequalities:

$$\bar{P}_{li} \leq \bar{P}^*_i \leq \bar{P}_{ui}, \forall i \in [1, N], \tag{8}$$

where $\bar{P}_{li}$ and $\bar{P}_{ui}$ refer to the lower and upper active power limits of the ith SM, respectively, while $\bar{P}^*_i$ denotes the power reference of the ith SM. Note that $\bar{P}_{li}$ and $\bar{P}_{ui}$ can differ among the SMs in a hybrid BESS. Violating the hardware constraints compromises the converter safety and operation.

2) Summation Constraint: The sum of the SM active power references must be equal to the total active power reference of the BESS, denoted as $\bar{P}^*_{BESS}$. Thus, the summation constraint corresponds to the following equality:

$$\sum_{i=1}^{N} \bar{P}^*_i = \bar{P}^*_{BESS}. \tag{9}$$

3) Disparity Constraints: According to the analysis in [23], [24], there are constraints on the disparity among the SM active power references, i.e., there is an upper limit in the active power that can be processed by a certain number of SMs. The disparity constraints can be formulated as [23]

$$\sum_{j=1}^{n} \bar{P}^*_j \leq \bar{P}^n_{max}, \forall n \in [1, N-1], \tag{10}$$

where $\bar{P}^*_j$ refers to the jth ($j \in [1, N]$) maximum active power reference, $\sum_{j=1}^{n} \bar{P}^*_j$ refers to the sum of the n largest power references, and $\bar{P}^n_{max}$ denotes the maximum active power that can be processed by the n SMs. Note that $\bar{P}^*_j$ is different from $\bar{P}^*_i$, as $\bar{P}^*_i$ refers to the power reference of the ith SM. The derivation of $\bar{P}^n_{max}$ is explained in [23], [24] and hence not repeated in this paper for the sake of simplicity. The value of $\bar{P}^n_{max}$ is determined by the SM capacitor voltage, the converter output voltage and arm current. Unlike the hardware constraints, violating the disparity constraints involves unfeasible power references, i.e., the SMs will fail to track their corresponding power references, thus limiting the converter operation.

B. Unconstrained SoC Balancing Solution

This subsection explains how to calculate the active power reference for each SM that can balance their SoC values with consideration of the summation constraint (9). The hardware and disparity constraints will be incorporated in the subsequent stages.

From (3) and (4), the average battery current of a SM depends on the SM active power as:

$$\bar{i_i} = \frac{\eta_i \bar{P}_i}{V_{bi}}. \tag{11}$$

Combining (1) and (11), the SoC dynamics correspond to

$$\dot{SoC}_i(t) = \frac{\eta_i \bar{P}_i}{Q_i V_{bi}}, \tag{12}$$

Hence, the SoC values can be balanced via a proper allocation of the SM active power references.

To balance the SoC, the proposed method aims at steering the SoC of all the SMs to a prescribed reference value, SoC^*, simultaneously. From (12), when the ith SM is charged with a certain active power $\bar{P}_i$, the time for its SoC value to reach SoC^* will be

$$t_i = \frac{SoC^* - SoC_i}{\dot{SoC}_i}. \tag{13}$$

Substituting (12) into (13), it is derived that

$$t_i = \frac{E_i}{\bar{P}_i}, \tag{14}$$

where

$$E_i = \frac{(SoC^* - SoC_i) Q_i V_{bi}}{\eta_i}. \tag{15}$$

Note that E_i corresponds to the energy required to steer SoC_i to SoC^*.

As the battery modules of all the SMs are expected to reach their corresponding SoC^* simultaneously, t_i should be similar for all the SMs:

$$\frac{E_i}{\bar{P}_i} = T_C, \forall i \in [1, N], \tag{16}$$

where $T_C > 0$ refers to the time to steer SoC_i to SoC^* for all the SMs. Combining (16) and the summation constraint in (9), the active power reference of each SM corresponds to

$$\bar{P}_i^* = \frac{E_i}{\sum_{i=1}^{N} E_i} \bar{P}_{BESS}^*. \tag{17}$$

Note that in the proposed method, the SoC balancing speed is affected by the value of SoC^*. According to (15) and (17), (16) is rewritten as

$$T_C = \frac{1}{\bar{P}_{BESS}^*} \sum_{i=1}^{N} \frac{(SoC^* - SoC_i(0)) Q_i V_{bi}}{\eta_i}, \tag{18}$$

where $SoC_i(0)$ refers to the initial SoC value. Hence, if there is a desired T_C, the value of SoC^* can be calculated by solving (18). When there is no specific requirement of T_C, SoC^* can be simply chosen as the allowed maximum SoC value (SoC_U) when $\bar{P}_{BESS}^* > 0$ and simply chosen as the allowed minimum SoC value (SoC_L) when $\bar{P}_{BESS}^* < 0$, which guarantees that the batteries in all the SMs can be fully charged/discharged simultaneously.

C. Hardware Constraints Incorporation

If the unconstrained SM active power references calculated according to (17) are outside the range $[\bar{P}_{li}, \bar{P}_{ui}]$ defined by (8), the hardware constraints are violated. In this condition, the SM active power references should be modified for a safe operation.

Assume that there are some power references higher than their corresponding upper bounds, whose indices i are grouped in the set X, and some power references lower than their corresponding lower bounds, whose indices i are grouped in the set Y, i.e.:

$$\begin{aligned} &\bar{P}_i^* > \bar{P}_{ui}, \forall i \in X, \\ &\bar{P}_i^* < \bar{P}_{li}, \forall i \in Y, \\ &\bar{P}_{li} \le \bar{P}_i^* \le \bar{P}_{ui}, \forall i \notin X \cup Y. \end{aligned} \tag{19}$$

To satisfy the hardware constraints, the power references that are outside the range will be saturated to their corresponding bounds, i.e., $\bar{P}_{li}$ or $\bar{P}_{ui}$. This changes the sum of the power references. Hence, to compensate for this change and thus keep the sum of power references equal to $\bar{P}_{BESS}^*$ in (9), an opposite change, denoted as $\Delta\bar{P}_h^*$, must be shared by the power references

$$\Delta\bar{P}_h^* = \sum_{i \in X} (\bar{P}_{ui} - \bar{P}_i^*) + \sum_{i \in Y} (\bar{P}_{li} - \bar{P}_i^*). \tag{20}$$

If $\Delta\bar{P}_h^* > 0$, which means that the power references need to be increased, $\Delta\bar{P}_h^*$ will be shared by those references that are below their upper bounds. Similarly, if $\Delta\bar{P}_h^* < 0$, $\Delta\bar{P}_h^*$ will be shared by those references that are above their lower bounds. A straightforward method would be to distribute $\Delta\bar{P}_h^*$ evenly among the power references. However, this even distribution cannot guarantee that the updated power references are within the safe range $[\bar{P}_{li}, \bar{P}_{ui}]$. For this reason, a method is proposed to distribute $\Delta\bar{P}_h^*$ according to the increase and decrease margins of the power references. The method aims at penalizing more the power references that are far from their corresponding bounds, while penalizing less the references that are close to their bounds. The increase and decrease margins of the ith SM correspond to:

$$IM_i = \bar{P}_{ui} - \bar{P}_i^*, \tag{21}$$

$$DM_i = \bar{P}_i^* - \bar{P}_{li}, \tag{22}$$

respectively.

If $\Delta\bar{P}_h^* > 0$, $\Delta\bar{P}_h^*$ will be distributed among the references according to their increase margins. Hence, each SM power reference will be increased by

$$\Delta\bar{P}_{hi}^* = \frac{IM_i}{\sum_{i=1}^{N} IM_i} \Delta\bar{P}_h^*. \tag{23}$$

Note that $\Delta\bar{P}_{hi}^*$ will be zero for those SMs whose active power references have reached their upper bounds since they cannot be further increased ($IM_i = 0$). Similarly, if $\Delta\bar{P}_h^* < 0$, each power reference will be decreased by:

$$\Delta\bar{P}_{hi}^* = \frac{DM_i}{\sum_{i=1}^{N} DM_i} \Delta\bar{P}_h^*, i \in [1, N]. \tag{24}$$

Note that $\Delta\bar{P}^*_{hi}$ will be zero for those SMs whose active power references have reached their lower bounds since they cannot be further decreased ($DM_i = 0$).

D. Disparity Constraints Incorporation

Once the hardware constraints have been incorporated, then the SM power references need to be assessed in terms of the disparity constraints in (10). The updated SM power references according to (23) or (24) are firstly sorted in descending order, and then evaluated in (10) from $n = 1$ to $n = N - 1$. If the power references satisfy the $N - 1$ inequalities in (10), they can be allocated to the corresponding SMs. Otherwise, they need to be modified as follows.

As a general case, let us assume that the disparity constraints in (10) are satisfied for the $m-1$ largest power references but violated for the m largest power references, which means

$$\begin{aligned}&\sum_{j=1}^{n}\bar{P}^*_j \le \bar{P}^n_{max}, \forall n \in [1, m-1],\\ &\sum_{j=1}^{m}\bar{P}^*_j > \bar{P}^m_{max}.\end{aligned} \tag{25}$$

Hence, to satisfy the disparity constraint when $n = m$, the m largest power references need to be reduced by at least

$$\Delta\bar{P}_d = \sum_{j=1}^{m}\bar{P}^*_j - \bar{P}^m_{max}, \tag{26}$$

where $\Delta\bar{P}_d > 0$. Accordingly, the remaining $N - m$ lowest power references need to be increased by $\Delta\bar{P}_d$ to guarantee that the sum of power references remains unchanged and equal to $\bar{P}^*_{BESS}$ in (9). For the sake of distinction, in this subsection the m largest power references are denoted as $\bar{P}^*_{j1}$, while the remaining $N-m$ lowest power references are denoted as $\bar{P}^*_{j2}$. Thus, $j1 \in [1, m]$ and $j2 \in [m + 1, N]$.

There are multiple methods to distribute the decrease of $\Delta\bar{P}_d$ among the m largest references $\bar{P}^*_{j1}$. However, to avoid violating the lower bounds of the hardware constraints, $\Delta\bar{P}_d$ will be distributed among the m references according to their corresponding decrease margins DM_{j1} in (22). Hence, $\bar{P}^*_{j1}$ will be updated as

$$\widehat{P}^*_{j1} = \bar{P}^*_{j1} - \Delta\bar{P}_d\frac{DM_{j1}}{\sum_{j1=1}^{m}DM_{j1}}, j1 \in [1, m], \tag{27}$$

where $\widehat{P}^*_{j1}$ represents the updated power reference of the $j1$th SM. Since $\Delta\bar{P}_d > 0$, the updated references $\widehat{P}^*_{j1}$ are below their corresponding original values $\bar{P}^*_{j1}$, i.e.:

$$\widehat{P}^*_{j1} \le \bar{P}^*_{j1}, \forall j1 \in [1, m]. \tag{28}$$

Note that the values of $\bar{P}^n_{max}$ are dependent on the operating condition of the converter and are not affected by the active power references of the SMs. Hence, as the original references $\bar{P}^*_{j1}$ satisfied the disparity constraints for $n \in [1, m-1]$, so will the updated references $\widehat{P}^*_{j1}$. Moreover, according to (26) and (27), the updated references $\widehat{P}^*_{j1}$ satisfy the disparity constraint in (10) for $n = m$, as their sum is saturated to $\bar{P}^m_{max}$, i.e.,

$$\sum_{j1=1}^{m}\widehat{P}^*_{j1} = \bar{P}^m_{max}. \tag{29}$$

After the m largest references ($\bar{P}^*_{j1}$) have been updated, the remaining references ($\bar{P}^*_{j2}$) should be updated to remain the total active power unaffected. The increase of $\Delta\bar{P}_d$ will be distributed among the remaining power references ($\bar{P}^*_{j2}$) according to their corresponding increase margins IM_{j2}. However, in this case, IM_{j2} of a SM is not only decided by the upper bound of its hardware constraint ($\bar{P}_{uj2}$), but also by the disparity constraints, as the disparity constraint can be violated when increasing a specific power reference. Note that this consideration is not needed when decreasing $\bar{P}^*_{j1}$ in (27) since decreasing power references does not compromise the disparity constraints.

For a general updated reference $\widehat{P}^*_{j2}$, the hardware constraint in (8) requires

$$\widehat{P}^*_{j2} \le \bar{P}_{uj2}. \tag{30}$$

Furthermore, the disparity constraint in (10) for $n = m + 1$ requires the sum of any $m + 1$ references to be below $\bar{P}^{m+1}_{max}$. Hence, the sum of any updated power reference $\widehat{P}^*_{j2}$ and the m references $\widehat{P}^*_{j1}$ should be below $\bar{P}^{m+1}_{max}$, i.e.:

$$\widehat{P}^*_{j2} + \sum_{j1=1}^{m}\widehat{P}^*_{j1} \le \bar{P}^{m+1}_{max}, \forall j2 \in [m + 1, N]. \tag{31}$$

According to (29), (31) can be rewritten as

$$\widehat{P}^*_{j2} \le \bar{P}^{m+1}_{max} - \bar{P}^m_{max}. \tag{32}$$

Combining (32) and (30), the increase margins of references $\bar{P}^*_{j2}$ are derived as

$$IM_{j2} = \min(\bar{P}^{m+1}_{max} - \bar{P}^m_{max}, \bar{P}_{uj2}) - \bar{P}^*_{j2}. \tag{33}$$

Hence, $\bar{P}^*_{j2}$ will be updated as:

$$\widehat{P}^*_{j2} = \bar{P}^*_{j2} + \Delta\bar{P}_d\frac{IM_{j2}}{\sum_{j2=m+1}^{N}IM_{j2}}, j2 \in [m + 1, N]. \tag{34}$$

Note that since the increase/decrease to the SM power references in (27) and (34) may not be balanced, the descending order of the power references may change after an updating iteration, which could affect the satisfaction of the disparity constraints. If an updated reference $\widehat{P}^*_{j2}$ becomes larger than an updated reference $\widehat{P}^*_{j1}$, the disparity constraints for $n \in [1, m]$ in (10) can be violated as the m references $\widehat{P}^*_{j1}$ are not the largest power references. Therefore, to ensure the satisfaction of the disparity constraints after an iteration, $\widehat{P}^*_{j1}$ must remain the m largest power references, i.e.:

$$\widehat{P}^*_{j1} \ge \widehat{P}^*_{j2}, \forall j1 \in [1, m] \wedge \forall j2 \in [m + 1, N], \tag{35}$$

which in fact is fulfilled by the proposed method, and the proof is provided next.

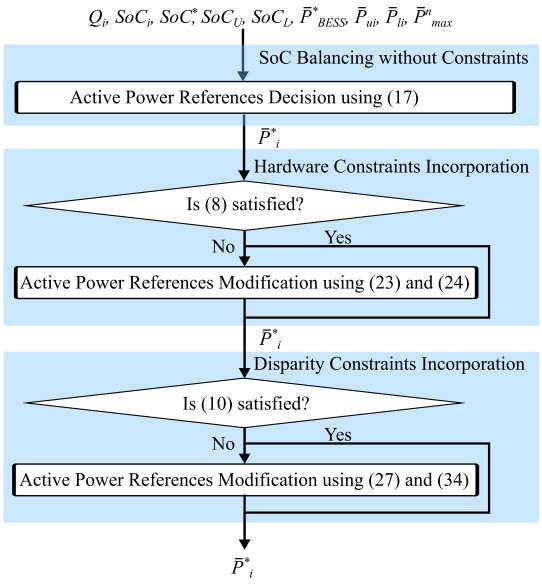

Fig. 3. Flowchart of the proposed rule-based SoC balancing method.

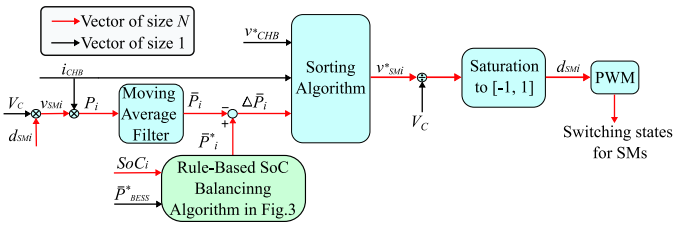

Fig. 4. SM power controller.

As discussed, the updated references $\widehat{P}^*_{j1}$ satisfies the disparity constraints in (10) for $n = m-1$, which means that the sum of any $m-1$ references among them is below $\bar{P}^{m-1}_{max}$:

$$(\sum_{j1=1}^{m} \widehat{P}^*_{j1}) - \widehat{P}^*_{j1} \leq \bar{P}^{m-1}_{max}, \forall j1 \in [1, m]. \tag{36}$$

Combining (36) and (29) yields

$$\widehat{P}^*_{j1} \geq \bar{P}^m_{max} - \bar{P}^{m-1}_{max}, \forall j1 \in [1, m]. \tag{37}$$

Besides, according to (32), each updated reference $\widehat{P}^*_{j2}$ is below $\bar{P}^{m+1}_{max} - \bar{P}^m_{max}$. According to the existing analysis in [25], it can be proved that:

$$\bar{P}^m_{max} - \bar{P}^{m-1}_{max} \geq \bar{P}^{m+1}_{max} - \bar{P}^m_{max}. \tag{38}$$

Combining (32), (37) and (38), it can be proved that (35) is true.

To conclude, the overall flowchart of the proposed rule-based SoC balancing method, which calculates the SM active power references with consideration of the active power constraints, is depicted in Fig. 3. After the calculation of SMs active power references, a controller is required to regulate the SM active power.

In this paper, the SM active power controller proposed in [23] is applied, which is depicted in Fig. 4. In this controller, a moving average filter is first used to calculate the average active power of each SM in a fundamental voltage period, denoted as $\bar{P}_i$. By comparing $\bar{P}_i$ with the corresponding references, the active power error is derived and denoted as $\Delta\bar{P}_i$. Based on $\Delta\bar{P}_i$, v^*_{CHB}, and i_{CHB}, a sorting stage is used to decide the output voltage reference of each SM (v^*_{SMi}). With the knowledge of v^*_{SMi}, a pulse width modulation (PWM) technique is applied to decide the switching state of each SM. Note that the major contribution of this paper is the rule-based SoC balancing method, which provides the active power references of the SMs.

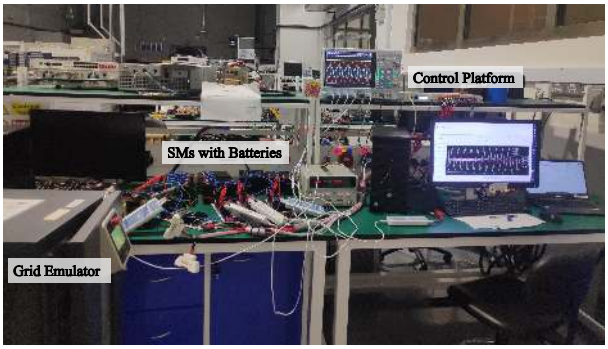

Fig. 5. Photo of the experimental prototype.

TABLE I
PARAMETERS OF THE EXPERIMENTAL BESS

Parameter	Value
Number of SMs per arm, N	4
SM capacitor voltage, V_C	50 V
SM capacitance, C	5 mF
Filter inductance, L	5 mH
Nominal output voltage (Peak), V_o	$110\sqrt{2}$ V
Nominal output current (Peak), I_{CHB}	$10\sqrt{2}$ A
Nominal output power, S_{nom}	1.1 kVA
Fundamental frequency, f	50 Hz

IV. EXPERIMENTAL RESULTS

To verify the performance of the proposed SoC balancing method, experimental results are obtained on a hybrid BESS, where the capacity of battery modules are considerably different among the SMs. The CHB converter is built with Imperix PEH 2015 full-bridge power modules and connected to the Cinergia grid emulator through a filtering inductor. The

TABLE II
PARAMETERS OF BATTERY MODULES

Parameter	Allowed Power Range, $[\bar{P}_{li}, \bar{P}_{ui}]$	Allowed SoC Range	Capacity
Base value	1.1 kVA	1	7 Ah
SM1	$[-33\%, 15\%]$	$[20\%, 80\%]$	100%
SM2	$[-33\%, 15\%]$	$[20\%, 80\%]$	90%
SM3	$[-33\%, 15\%]$	$[20\%, 80\%]$	80%
SM4	$[-33\%, 15\%]$	$[20\%, 80\%]$	70%

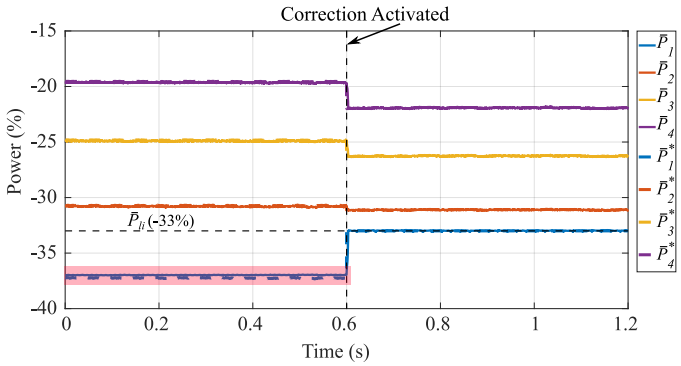

Fig. 6. ***Case I***: Power references and measured powers of each SM when the hardware constraints are violated.

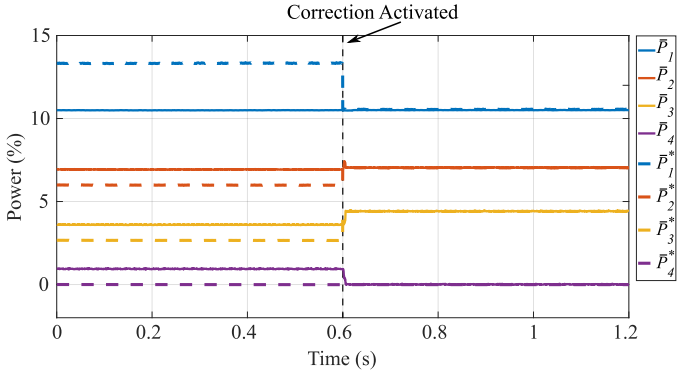

Fig. 7. ***Case II***: Power references and measured powers of each SM when the disparity constraints are violated.

Imperix B-Box RCP control platform is used to implement the control scheme. A picture of the setup is provided in Fig. 5. Parameters of the converter and battery modules are provided in Tables I and II, respectively.

A. Performance of the Proposed Method

To verify the performance of the proposed rule-based method, three different cases are tested in the experiments.

Case I: The first case investigates the ability of the proposed method to correct the power references when the hardware constraints are violated. In this specific case, the BESS is discharged with nominal power. The initial SoC values from SM1 to SM4 are 51.2%, 51.1%, 51.0%, and 50.9%, respectively. The power reference and measured active power of each SM are provided in Fig. 6. Before the activation of the power references correction at t =0.6 s, as highlighted with red shading in the figure, the power reference and measured active power of SM1 are lower than its lower hardware limit ($\bar{P}_{l1} = -33\%$), which compromises the converter safe operation. After the activation, the active power reference of SM1 is increased and saturated at its lower limit, while the power references of the remaining SMs are decreased accordingly, which maintains the total active power of the BESS and avoids discharging the SM1 excessively. Furthermore, as observed, the decrease of active power references is distributed among the SMs according to their corresponding decrease margins (DM_i). For instance, the

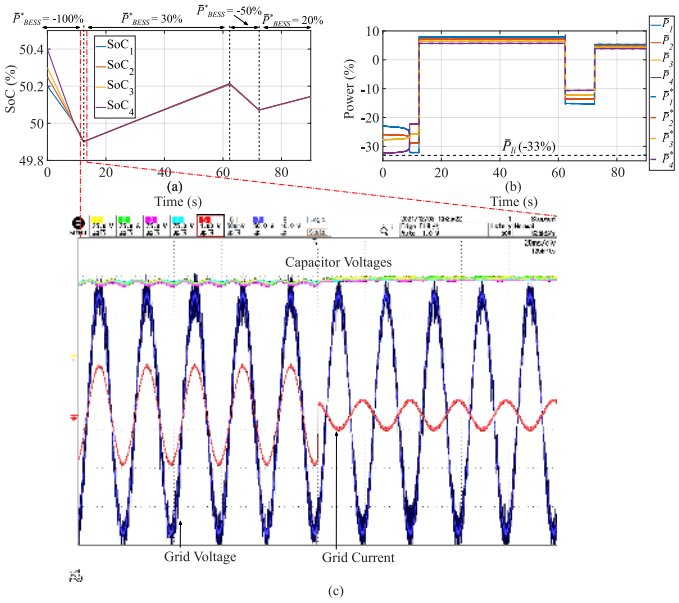

Fig. 8. ***Case III***: Experimental results when the BESS is charged and discharged consecutively: (a) SoC of each SM, (b) power references and measured powers of each SM, and (c) recorded capacitor voltages, grid voltage and current in the oscilloscope.

active power reference of SM4 decreases the most as its DM_i is the highest. This effectively guarantees that the updated power references do not violate the hardware constraints.

Case II: The second case investigates the ability of the proposed method to correct the power references when the disparity constraints are violated. The BESS is charged with 25% of the nominal power. The initial SoC values from SM1 to SM4 are 79.2%, 79.6%, 79.8%, and 80.0%, respectively. The power reference and measured active power of each SM are provided in Fig. 7. Before the activation of power reference correction at t =0.6 s, all the SMs fail to track their corresponding power references because they violate the disparity constraints. Moreover, although the SoC of SM4 has reached the allowed upper limit (80%), this SM is charging because it fails to track its power reference. After the activation, the SM power references are modified and the updated power references satisfy the disparity constraints. As observed, the measured power of each SM tracks its corresponding reference and SM4 is not charging.

Case III: The third case investigates the ability of the proposed method to balance the SoC values when the BESS is charged and discharged with different active power values consecutively. The results are provided in Fig. 8. According to Fig. 8(a), the SoC values of all the SMs reach balance at approximately t = 9 s, and then remain balanced despite the change of the BESS power. According to Fig. 8(b), each SM effectively tracks its corresponding active power reference and the SM active power is regulated within the safe range $[-33\%, 15\%]$. Fig. 8(c) depicts the recorded capacitor voltages, grid voltage and arm current in the oscilloscope when the BESS power changes from -100% (discharge) to 30% (charge).

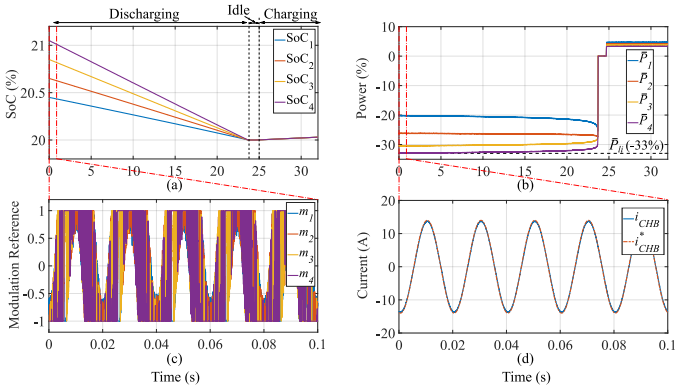

Fig. 9. Experimental results with the proposed rule-based method: (a) SoC of each SM, (b) measured active powers of each SM, (c) modulation reference, and (d) arm current.

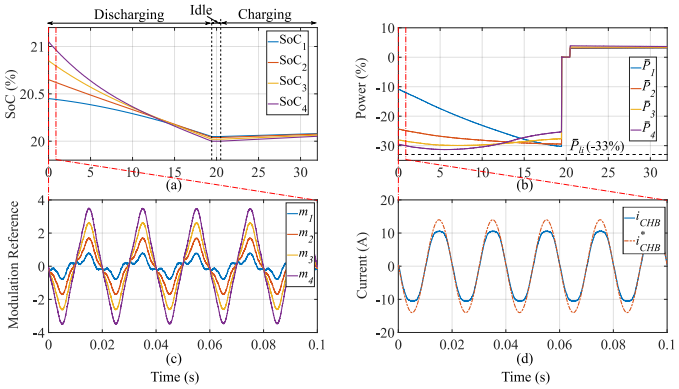

Fig. 11. Experimental results of the PI-based method with overmodulation: (a) SoC of each SM, (b) measured active powers of each SM, (c) modulation reference, and (d) arm current.

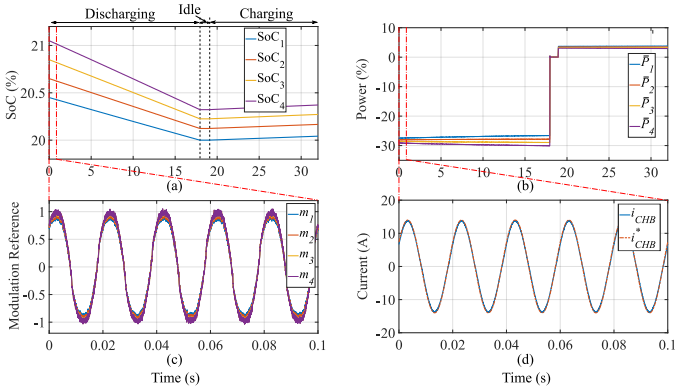

Fig. 10. Experimental results of the PI-based method without overmodulation: (a) SoC of each SM, (b) measured active powers of each SM, (c) modulation reference, and (d) arm current.

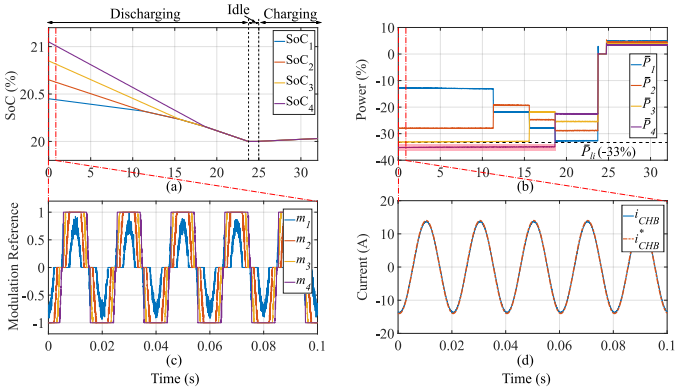

Fig. 12. Experimental results with the sorting-based method: (a) SoC of each SM, (b) measured active powers of each SM, (c) modulation reference, and (d) arm current.

To conclude, the proposed rule-based method can simultaneously balance the SoC values and regulate the SM active powers within a prescribed safe range.

B. Comparison with Different SoC Balancing Methods

This subsection compares the performances of the proposed method and the conventional methods. The BESS is firstly discharged with the nominal power and then charged with 20% of the nominal power. Results are provided in Figs. 9, 10, 11, and 12. The initial SoC values are unbalanced among the SMs.

Fig. 9 presents the results when the proposed rule-based method is implemented. Fig. 9(a) shows the SoC values of the SMs. As observed, the SoC values of all the SMs reach balance by the end of the discharging period. The active powers of the SMs are provided in Fig. 9(b), which are within their safe range. Fig. 9(c) provides the modulation references of each SM, which consist of some other harmonic components besides the fundamental one. Nevertheless, the harmonics cancel out, and hence the arm current of the CHB converter effectively tracks its reference, as Fig. 9(d) shows.

Fig. 10 presents the results when the PI-based method is implemented. The SM active powers are within the safe range and the arm current is well regulated, as observed from Figs. 10(b) and (d), respectively. However, according to Fig. 10(a), the SoC values do not reach balances. The SoC of the SM1 reached the allowed lower limit (20%) earlier than the remaining SMs and hence, the discharging process ends in advance without fully discharging the batteries. Note that in this case the PI controller is tuned to maximize the SoC balancing capability without causing overmodulation. As shown in Fig. 10(c), the modulation reference of SM1 has been maximized within [-1, 1]. These results show the reduced SoC balancing capability of the PI-based method.

The PI parameters can be further increased to pursue a better SoC balancing performance, and the results are provided in Fig. 11. According to Figs. 11(a) and (b), a better SoC balance is achieved and the SM active powers are still within the safe range. However, overmodulation occurs in SMs 2, 3 and 4, as shown in Fig. 11(c). Consequently, the arm current cannot be regulated to its reference, as shown in Fig. 11(d).

Fig. 12 presents the results when the sorting-based method is implemented. As observed, the SoC balance is achieved, overmodulation is avoided, and the arm current is effectively regulated. However, the active power of SM1 is lower than its lower hardware limit during the discharging period, which is highlighted with red shading in Fig. 12(b).

A comparison of the computational burden among the

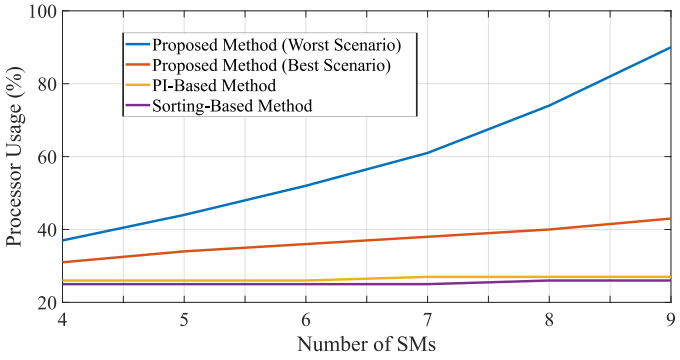

Fig. 13. Comparison of the computational burden between the existing and proposed methods.

TABLE III
COMPARISON OF THE SOC BALANCING METHODS.

	Proposed	PI 1	PI 2	Sorting
SoC Balance Capability	High	Low	Low	High
Total Harmonic Distortion	Low	Low	High	Low
Computational Burden	High	Low	Low	Low
Power Constraints Satisfaction	Yes	No	No	No

methods is conducted on the control platform. The processor usage of the control platform is selected as the indicator of the computational burden and the results are provided in Fig. 13. Note that the worst scenario of the proposed method means that the originally preferred SM power references violate all the hardware and disparity constraints, while the best scenario means the original power references satisfy all the constraints. From Fig. 13, the computational burden of the proposed method is heavier than the existing methods. This is because the proposed method needs to check the satisfaction of the different constraints, and modify the references when needed. If the proposed control method does not perform this correction duty, the system safety and operation are jeopardized, which is not desirable.

To conclude the experimental results, only the proposed rule-based method can balance the SoC without compromising the BESS operation, although it has a higher computational burden.

A brief comparison of all the SoC balancing methods studied in this paper is shown in Table III, where the PI 1 and 2 correspond to the PI-based methods with and without overmodulation, respectively.

V. CONCLUSION

A rule-based method has been proposed to balance the SoC among the SMs within one arm of the CHB converter-based BESS. Compared to the conventional methods, the major advantage of the proposed algorithm is its ability to consider the SM active power constraints without compromising the SoC balancing performance. Moreover, the proposed method can consider the differences among battery modules, hence it is applicable to hybrid BESS applications. Experimental results have confirmed the effectiveness of the proposed algorithm and have shown its advantages compared to the conventional methods.

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