A Predictive Capacitor Voltage Control of a Hybrid Cascaded Multilevel Inverter With a Single DC Link and Reduced Common Mode Voltage Operation

Arun Rahul S, R. Sudharshan Kaarthik, *Student Member, IEEE*, K. Gopakumar, *Fellow, IEEE*, Leopoldo G. Franquelo, *Fellow, IEEE* and Jose I. Leon, *Senior Member, IEEE*

***Abstract*—For cascaded multilevel inverter topologies with a single DC supply, closed loop capacitor voltage control is necessary for proper operation. This paper presents zero and reduced common mode voltage (CMV) operation of a hybrid cascaded multilevel inverter with predictive capacitor voltage control. Each phase of the inverter is realized by cascading two 3-level flying capacitor inverters with a half bridge module in between. For the presented inverter topology, there are redundant switching states for each inverter voltage levels. By using these switching state redundancies, for every sampling instant, a cost function is evaluated based on the predicted capacitor voltages for each phase. The switching state which minimizes cost function is treated as the best and is switched for that sampling instant. The inverter operates with zero CMV for a modulation index upto 86%. For modulation indices from 86% to 96% the inverter can operate with reduced CMV magnitude (Vdc/18) and reduced CMV switching frequency using the new space-vector PWM (SVPWM) presented herein. As a result, the linear modulation range is increased to 96% as compared to 86% for zero CMV operation. Simulation and experimental results are presented for the inverter topology for various steady state and transient operating conditions by running an induction motor drive with open loop V/f control scheme.**

***Index Terms*—Predictive Control, Induction motor drive, PWM, Multilevel inverter, Common mode voltage, Floating capacitor**

I. Introduction

MULtilevel inverters result in reduced voltage harmonic distortion and are ideal for low switching frequency high performance medium voltage applications [1], [2]. Commonly used multilevel inverter topologies are Neutral Point Clamped inverter (NPC) [3], Flying Capacitor inverter (FC) [4]–[6], Cascaded H-Bride inverter (CHB) [7], [8], and hybrid topologies [9], [10]. Hybrid cascaded inverter topologies [10], [12], [13] result in more voltage levels with reduced number of DC supplies and semiconductor devices compared to NPC, FC and CHB.

Manuscript received June 15, 2015; revised October 15, 2015 and January 25, 2016; accepted February 25, 2015.

Arun Rahul S and K. Gopakumar are with the Department of Electronic Systems Engineering (Formerly Centre for Electronics Design and Technology), Indian Institute of Science, Bangalore-560012, India. e-mail: kgopa@dese.iisc.ernet.in.

R. Sudharshan Kaarthik is with Concordia University, Canada.

Jose I. Leon and Leopoldo G. Franquelo is with the Department of Electronics Engineering, University of Seville, 41004, Seville, Spain.

In recent years, model predictive control (MPC) has proved to be a good choice for the control of power converter and motor drive applications [3], [9], [14]. MPC predicts system behaviour using a system model and current system state. For multilevel inverters, which have a finite number of switching states, a predictive controller can select the best state from a number of possible states. A cost function is evaluated for each of the finite states and the state which minimizes the cost function is used for operation. When number of finite states of the system increases, the computation process also increases for predictive control. In [7], a high dynamic performance predictive control algorithm with reduced computations is presented for an asymmetric cascaded H-bridge inverter. In [8], a predictive current controller for cascaded H-bridge inverter with reduced computations is presented. FPGA based implementations of MPC algorithms for NPC and CHB inverter topologies are presented in [15] and [16] respectively. In [17], predictive control algorithm is used to minimize the circulating current and balance the DC bus voltage of a modular multilevel inverter topology.

Reduced or zero CMV operation is desirable for voltage source inverter fed motor drives to avoid motor bearing failure [18], [19]. By using a modified PWM switching technique [20], for a two level inverter, the effect of CMV and common mode current (motor bearing current) can be reduced. In multilevel inverter fed motor drive applications, it is possible to make the CMV zero. This is done by selecting voltage space vectors with zero CMV for synthesizing the reference voltage [10], [21], [22]. The disadvantage of zero CMV operation is the reduction in linear modulation range compared to that of normal inverter operation. In [11], a SVPWM technique is presented to extend the linear modulation range of multilevel inverters with reduced CMV switching.

In this paper, a cascaded multilevel inverter with a single DC supply is operated with zero and reduced common-mode voltage with a predictive capacitor voltage controller. Floating capacitors are used for generating the multiple voltage levels. A cost function is evaluated separately for each phase of the inverter to reduce computation time. Also zero and reduced CMV operation of the inverter with SVPWM technique is analysed. A new space vector PWM technique is proposed for the first time with a reduced CMV magnitude ($V_{dc}/18$) and reduced CMV switching frequency (three times the fun-

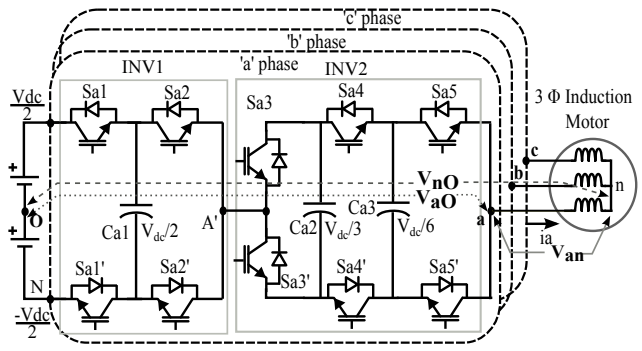


Fig. 1. Power circuit for the hybrid seven level inverter topology. $V_{aO}$is defined as inverter pole voltage (voltage between inverter pole 'a' and DC bus mid point 'O'), $V_{an}$is defined as motor phase voltage (voltage between inverter pole 'a' and DC motor neutral 'n') and $V_{nO}$is defined as common mode voltage (voltage between motor neutral 'n' and DC bus mid point 'O').

damental frequency). Using this technique, 10% increase in the linear modulation range is achieved compared to zero CMV operation, resulting in improved DC bus utilization.

II. Inverter Topology

Fig. 1 shows the power circuit of a hybrid cascaded multilevel inverter with a single DC supply. The topology consists of five pairs of complementary switches with 32 (2^5) switching states for each phase. The switches Sx1, Sx2, Sx3, Sx4, Sx5 and Sx1$'$, Sx2$'$, Sx3$'$, Sx4$'$, Sx5$'$ respectively (x = a, b, c phases) are operated in a complementary manner (Sx1 = 1 implies Sx1 is ON and Sx1$'$ is OFF). The three capacitors (Cx1, Cx2 and Cx3) per phase are maintained at voltages $V_{dc}/2$, $V_{dc}/3$, and $V_{dc}/6$ respectively. Each phase of the topology can be analysed as a cascaded combination of three-level flying capacitor inverter with a modified five-level flying capacitor inverter. This combination of three level and five level inverters can generate eleven voltage levels at 'a', 'b' and 'c' with respect to DC bus mid point 'O'. Seven out of these 11 levels can control capacitor voltages over a switching cycle irrespective of the load power factor and modulation index. This feature can be used for reducing the capacitor size for a given power level. For each of these seven levels, Table I shows the redundant switching states and effect of these switching states on capacitor charge for a given current direction for phase 'a'. It can be noted that for pole voltage levels $-V_{dc}/2$ and $V_{dc}/2$, all capacitors of that phase are bypassed and hence the voltages are unaffected. For pole voltage levels $-V_{dc}/3$, 0, and $V_{dc}/3$, there are four redundant switching states, and for pole voltage levels $-V_{dc}/6$ and $V_{dc}/6$, there are five redundant switching states. For the remaining four pole voltages ($-5V_{dc}/6$, $-4V_{dc}/6$, $4V_{dc}/6$ and $5V_{dc}/6$), the capacitor charging depends on both modulation index and load power factor. This imposes operating limit for the stable operation of inverter and requires special control algorithms to maintain the capacitor voltage. So these pole voltages are not used for the inverter operation presented in this work.

In SVPWM with hysteresis band based capacitor voltage control schemes, the capacitor voltages are compared to reference voltages in a hysteresis comparator. At each

TABLE I. INVERTER SWITCHING STATES AND EFFECT ON CAPACITOR CHARGING

Pole Voltage (V_{aO}) Levels	Method of Pole Voltage Generation	Status of switches	Capacitor charging status (i_a+ve)		
			$Vca1$	$Vca2$	$Vca3$
$-V_{dc}/2$	$-V_{dc}/2$	00XXX	U	U	U
$-V_{dc}/3$	$-V_{dc}/2+Vca3$	00001	U	U	D
	$-V_{dc}/2+Vca2-Vca3$	00010	U	D	C
	$-V_{dc}/2+Vca1-Vca2$	01100	D	C	U
	$-V_{dc}/2+V_{dc}-Vca1-Vca2$	10100	C	C	U
$-V_{dc}/6$	$-V_{dc}/2+Vca2$	00011	U	D	U
	$-V_{dc}/2+Vca1-Vca2+Vca3$	01101	D	C	D
	$-V_{dc}/2+Vca1-Vca3$	01110	D	U	C
	$V_{dc}/2-Vca1-Vca2+Vca3$	10101	C	C	D
	$V_{dc}/2-Vca1-Vca3$	10110	C	U	C
0	$-V_{dc}/2+Vca1$	01XXX	D	U	U
	$V_{dc}/2-Vca1$	10XXX	C	U	U
$V_{dc}/6$	$-V_{dc}/2+Vca1+Vca3$	01001	D	U	D
	$-V_{dc}/2+Vca1+Vca2-Vca3$	01010	D	D	C
	$V_{dc}/2-Vca1+Vca3$	10001	C	U	D
	$V_{dc}/2-Vca1+Vca2-Vca3$	10010	C	D	C
	$V_{dc}/2-Vca2$	11100	U	C	U
$V_{dc}/3$	$-Vdc/2+Vca1+Vca2$	01011	D	D	U
	$V_{dc}/2-Vca1+Vca2$	10011	C	D	U
	$V_{dc}/2-Vca2+Vca3$	11101	U	C	D
	$V_{dc}/2-Vca3$	11110	U	U	C
$V_{dc}/2$	$V_{dc}/2$	11XXX	U	U	U

Note1 : 'U' - capacitor charge is unaffected, 'C' - capacitor is charging, 'D'- capacitor is discharging and current flow from inverter to motor neutral 'n' is taken as positive.
Note2: Status of switch means status of Sa1, Sa2, Sa3, Sa4, Sa5 and 'X' can be either '0' or '1'

sampling instant, the controller selects the switching state from a look-up table based on the hysteresis outputs and desired pole voltage [21]. The controller does not consider the present value of capacitor voltage and phase current, and capacitor voltages may cross the hysteresis bands for some load conditions, resulting in higher capacitor voltage ripple. Further, the capacitor voltage dynamics are sensitive to the static look-up table entries.

III. Predictive Capacitor Voltage Control

In predictive control, capacitor voltages for the next sampling instant are predicted using the present capacitor voltages, phase currents and inverter switching functions. To control the dynamics of capacitor voltage, a cost function is evaluated using the predicted capacitor voltages for every redundant switching state. The switching state which minimizes the cost function is switched to generate the inverter pole voltage level. In predictive capacitor voltage control, out of the available switching states, the best state is used and hence capacitor voltage ripple is lower compared to a hysteresis band based

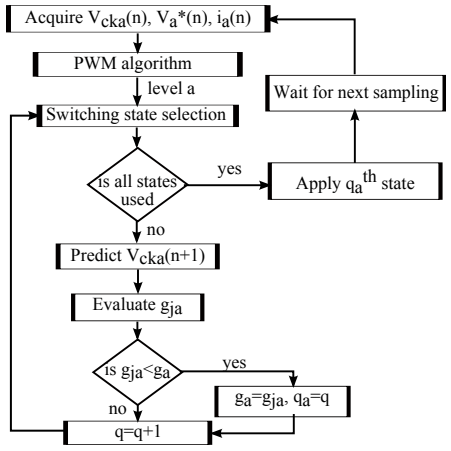


Fig. 2. Flowchart of predictive capacitor voltage controller.

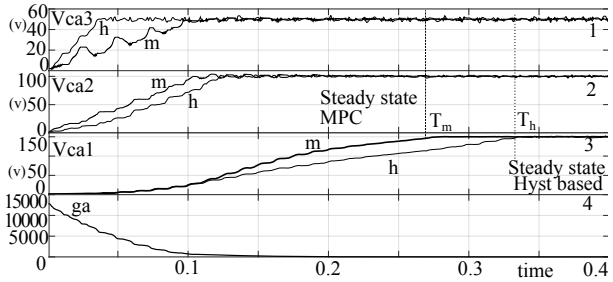


Fig. 3. Simulation results showing the voltage build-up of capacitors from a relaxed state of 0V for predictive control and hysteresis band based control. Wave forms shown are $V_{dc}/6$ capacitor voltage ($Vca3$), $V_{dc}/3$ capacitor voltage ($Vca2$), $V_{dc}/2$ capacitor voltage ($Vca1$) and and cost function (g_a) for phase 'a' (m - MPC, h - hysteresis band based control).

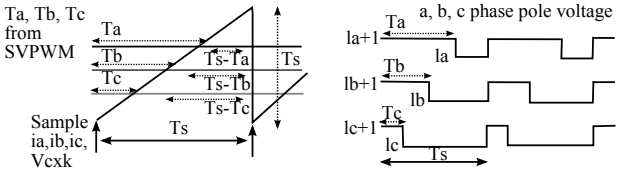
control. In [6], predictive control of a four level flying capacitor inverter using space vector redundancy is presented. A seven level hybrid inverter topology with predictive capacitor voltage control using space vector redundancies is proposed in [13]. A predictive current control for an asymmetric flying capacitor inverter with flying capacitor voltage ratio control is presented in [23].

For the cascaded inverter topology presented here, each phase of the topology is modelled using switching functions. The inverter pole voltage (V_{xO}) with respect to DC bus mid point 'O' for any phase is defined as,

$$V_{xO}(n+1) = Sx1V_{dc} - \frac{V_{dc}}{2} + \sum_{k=1}^{3} f_{xk}(sw)V_{cxk}(n+1) \quad (1)$$

where k = 1, 2 and 3, $f_{x1}(sw) = (Sx1 - Sx2)$, $f_{x2}(sw) = (Sx3 - Sx4)$, $f_{x3}(sw) = (Sx4 - Sx5)$, (Sx can be '0' or '1') and x = a, b, c. $V_{cxk}(n+1)$ is the kth capacitor voltage of xth phase for the (n+1)th sampling instant.

In this paper, zero and reduced CMV operation of a seven level inverter with SVPWM and predictive capacitor voltage control is presented. For controlling the dynamics, capacitor voltages needs to be predicted for every switching cycle. The information about the pole voltage levels to be switched and the time duration of each pole voltage levels to be applied can be obtained from the SVPWM algorithm. Fig. 4 shows the 'a', 'b' and 'c' phase timing signals and the pole voltage transitions



Note: 'lx 'can be 0, 1, 2, 3, 4, 5, 6 which corresponds to pole voltages -V_{dc}/2, -V_{dc}/3, -V_{dc}/6, 0, V_{dc}/6, V_{dc}/3, V_{dc}/2 and x = a, b, c.

Fig. 4. SVPWM timing signals and inverter pole voltage switching.

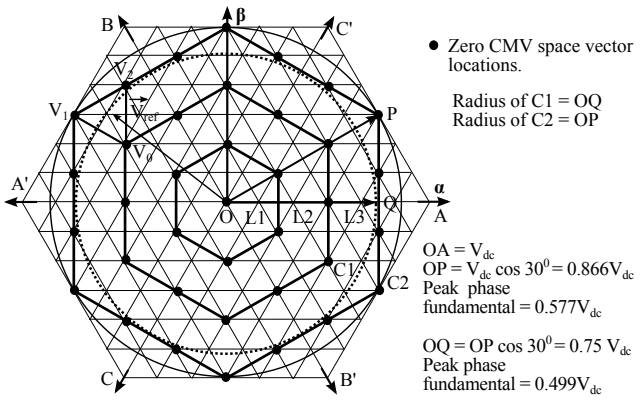


Fig. 5. Formation of a four level zero CMV space vector structure from a seven level space vector structure.

over a switching cycle 'Ts'. In general, with SVPWM, the inverter pole voltage of xth phase remains at level 'lx+1' for a duration of 'Tx' and at 'lx' for a duration of 'Ts-Tx'. Using capacitor voltages $V_{cxk}(n)$ and phase current i_x measured at n^{th} sampling instant along with the pole voltage level data and timing information, the capacitor voltage for the duration 'Tx' can be predicted as,

$$V_{cxk}(n+1) = V_{cxk}(n) + f_{xk}(sw)\frac{1}{C}\int_{nTs}^{(nTs+Tx)} i_x dt \quad (2)$$

By using the switching function $f_{xk}(sw)$, the capacitor voltages $V_{cxk}(n+1)$ for each redundant state can be obtained. The predicted voltage error for kth capacitor of xth phase at nth sampling instant can be,

$$\triangle V_{cxk} = V_{cxk}(n+1) - V_{cxkref}. \quad (3)$$

where V_{cxkref} is the reference voltage of kth capacitor of xth phase. The predictive capacitor voltage control uses a cost function. For zero CMV and reduced CMV operation, the cost function for each phase is evaluated separately. For each phase, by using a separate cost function, phase capacitors are controlled independently and ensures best switching state is selected for each phase. With individual cost function for each phase, the number of computation required also reduces. The number of computation required with single cost function will be (redundancy of 'a' × redundancy of 'a' × redundancy of 'c') compared to (redundancy of 'a' + redundancy of 'b' + redundancy of 'c') with individual cost function. The cost function for xth phase is defined as,

$$g_x = \frac{1}{2}C_{xk}[\triangle V_{cxk}][w_k][\triangle V_{cxk}]^T \quad (4)$$

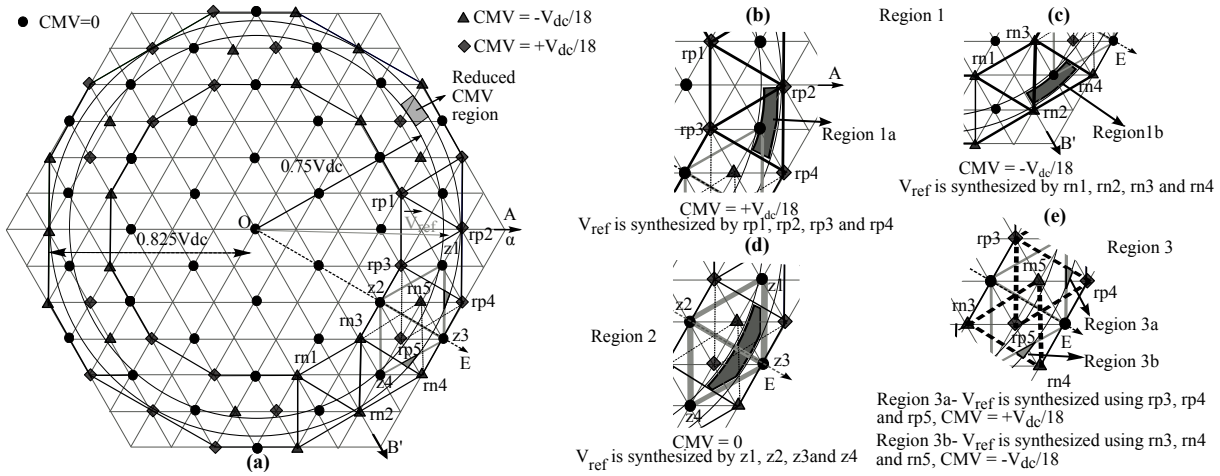


Fig. 6. Space vector structure showing reduced CMV space vector locations and the operating region is shown in between the inscribed circles.

where $[\triangle V_{cxk}] = [\ \triangle V_{cx1} \quad \triangle V_{cx2} \quad \triangle V_{cx3}]$ for x$^{\text{th}}$ phase and $[w_k] = \begin{bmatrix} w_1 & 0 & 0 \\ 0 & w_2 & 0 \\ 0 & 0 & w_3 \end{bmatrix}$ is a 3×3 weight matrix. The weight factor selection for a four level flying capacitor inverter is presented in [5]. The cost function is again defined as,

$$g_x = \frac{1}{2}\sum_{k=1}^{3} C_{xk} w_k (\triangle V_{cxk})^2 \tag{5}$$

Cost function g_x reaches zero when all the phase capacitors are charged to the reference values. The condition for minimum of the cost function is given by,

$$\frac{dg_x}{dt} = \sum_{k=1}^{3} C_{xk} w_k \triangle V_{cxk} \frac{dV_{cxk}(n+1)}{dt} \tag{6}$$

By evaluating the cost function for each switching state, the optimal switching state for the pole voltage level 'lx+1' can be obtained and all the capacitor voltages can be predicted for the duration 'Tx'. Using this information, optimal switching state for the pole voltage level 'lx' for the duration 'Ts-Tx' also can be obtained. The predictive capacitor voltage control algorithm implementation is described in the following steps and is shown as a flowchart in Fig. 2.

1) For nth sampling instant, using level shifted carrier based SVPWM, get the xth phase pole voltage level and timing information for inverter operation.
2) Predict (n+1)th instant capacitor voltage using SVPWM data, previous capacitor voltages and load current.
3) Evaluate the cost function g_x for all the possible switching states for the level data 'lx+1' and 'lx'. Find the switching state which minimizes the cost function g_x for each phase.
4) Apply the switching state for each phase and repeat the process from step 1 for next sampling instant.

Fig. 3 shows the convergence of cost function over time, during motor start-up with all capacitors for phase 'a' initially at 0V. The voltage build-up of capacitors from a relaxed state of 0V for predictive control and hysteresis control is also shown in Fig. 3. It can be seen that the steady state condition (i.e all capacitors are charged to reference) is reached faster with predictive controller than with a hysteresis controller.

IV. Seven Level Inverter Space Vector Structure and Zero CMV Locations

A seven level inverter has 343 (7^3) pole voltage combinations which are mapped to 127 space vector locations in the $\alpha - \beta$ plane. Out of these pole voltage combinations, 37 pole voltage combinations have zero common mode voltage with respect to motor neutral 'n' and DC bus midpoint 'O' ($V_{nO} = (V_{aO} + V_{bO} + V_{cO})/3$). Combining these zero CMV space vector locations, a four level inverter space vector structure rotated 30^0 anticlockwise is obtained as shown in the Fig. 5. The reference vector ($\overrightarrow{V_{ref}}$) is synthesized by averaging three adjacent vectors using (7 and 8). Analysing the zero CMV space vector structure, maximum peak of fundamental voltage possible is $0.499V_{dc}$ compared to $0.577V_{dc}$ with normal seven level inverter operation (for $0.577V_{dc}$, m = 1 and $0.499V_{dc}$, m = 0.86).

$$\overrightarrow{V_1}T_1 + \overrightarrow{V_2}T_2 + \overrightarrow{V_0}T_0 = \overrightarrow{V_{ref}}T_s \tag{7}$$

$$T_1 + T_2 + T_0 = T_s \tag{8}$$

V. Reduced CMV Operation to Extend Linear Modulation Range

As mentioned in the previous section, with zero CMV operation, DC bus utilization of the inverter gets reduced. In order to get the same torque capability for the induction motor operated with a normal seven level inverter, the DC link voltage needs to be increased for zero CMV operation. Instead of this, by allowing reduced common mode switching, DC bus utilization of inverter is improved compared to zero CMV operation. For the seven level inverter the next CMV near to zero is $\pm V_{dc}/18$ (Fig. 6). For reduced CMV operation presented in this paper, space vector triangles overlap in some regions. This conflict is solved by using the following method. To get minimum CMV switching over a fundamental cycle, the space vector locations are grouped in a special manner to synthesize the reference vector. Consider the 60^0 sector OAB', symmetric about the axis OE in Fig. 6. In the space

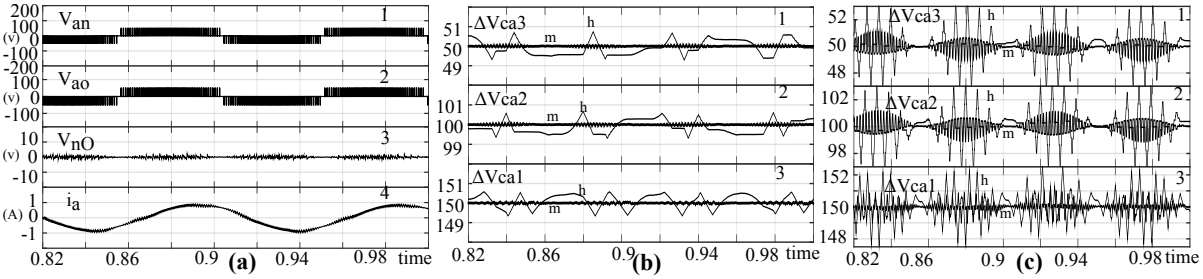


Fig. 7. Simulation results showing, Motor Phase voltage (V_{an}), Inverter pole voltage (V_{aO}), Common mode voltage (V_{nO}), Phase current (i_a) and capacitor voltage ripple (lightly shaded -1V hysteresis based control (h), dark shaded - MPC (m) for 10 Hz (m = 0.2) operation of inverter for phase 'a'.

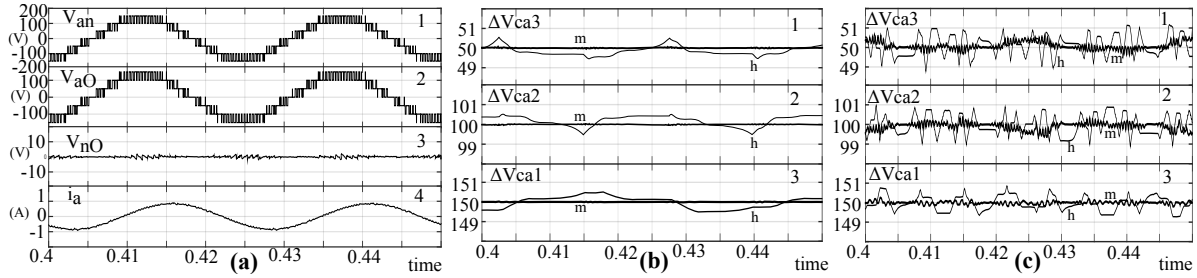


Fig. 8. Simulation results showing, Motor Phase voltage (V_{an}), Inverter pole voltage (V_{aO}), Common mode voltage (V_{nO}), Phase current (i_a) and capacitor voltage ripple (lightly shaded - 1V hysteresis based control (h), dark shaded - MPC (m)) for 40 Hz (m = 0.8) operation of inverter for phase 'a'.

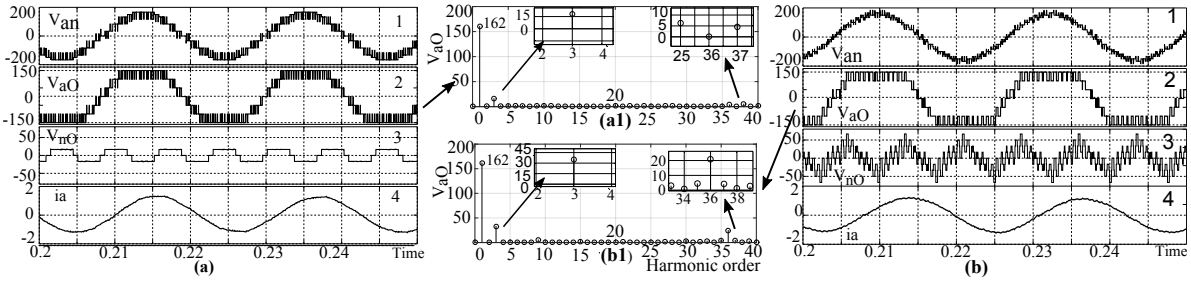


Fig. 9. Simulation results showing, 1) Motor Phase voltage (V_{an}), 2) Inverter pole voltage (V_{aO}), 3) Common mode voltage (V_{nO}), 4) Phase current (i_a) for a fundamental frequency of 45 Hz (m = 0.96) with reduced CMV operation and normal seven level operation of inverter.

vector structure, Region-1 is formed by the reduced CMV space vector locations rp1, rp2, rp3 and rp4 in the sub-sector AOE (Fig. 6(b)) and rn1, rn2, rn3 and rn4 in the sub-sector B'OE (Fig. 6(c)). Reference vector ($\overrightarrow{V_{ref}}$) is synthesized using nearest three vectors out of these vectors. Reference vector in Region-2 is synthesized using zero CMV space vector locations z1, z2, z3 and z4 (Fig. 6(d)). If the reference vector is in Region-3a, it is synthesized using rp3, rp4 and rp5 and in Region-3b, it can be synthesized using rn3, rn4 and rn5 (Fig. 6(e)). Same method applies for all the other 60^0 sectors. By using this method, the reference vector can be synthesized with only two CMV switching per 60^0 with a magnitude of $V_{dc}/18$. Using this SVPWM technique, maximum peak fundamental voltage possible is $0.55V_{dc}$, which is a 10% increase over zero CMV operation.

VI. Simulation and Experimental and Results

The inverter topology with predictive control is simulated in MATLAB-SIMULINK by modelling the inverter using switching functions. Induction motor is modelled with respect to stator axis reference frame. Various modulation techniques for multilevel power converters are presented in [24]. For

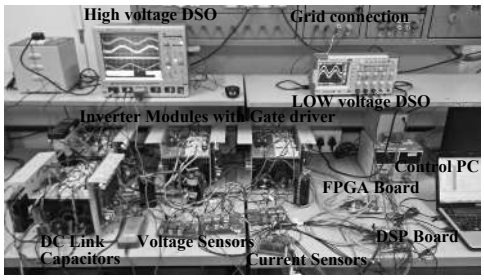


Fig. 10. Experimental setup showing the cascaded multilevel inverter and control boards.

zero CMV operation (m $\leq$ 0.866) presented here, a level shifted carrier based PWM algorithm [25] is used to get the space vector locations and PWM timings. For reduced CMV operation, PWM timings and space vector locations to be switched are obtained using a triangle search algorithm. This algorithm searches one by one all the triangles formed by nearest space vector locations in a sector for positive values of dwell times T0, T1 and T2.

The operation of inverter with predictive capacitor voltage control is tested on a 3 phase induction motor drive with

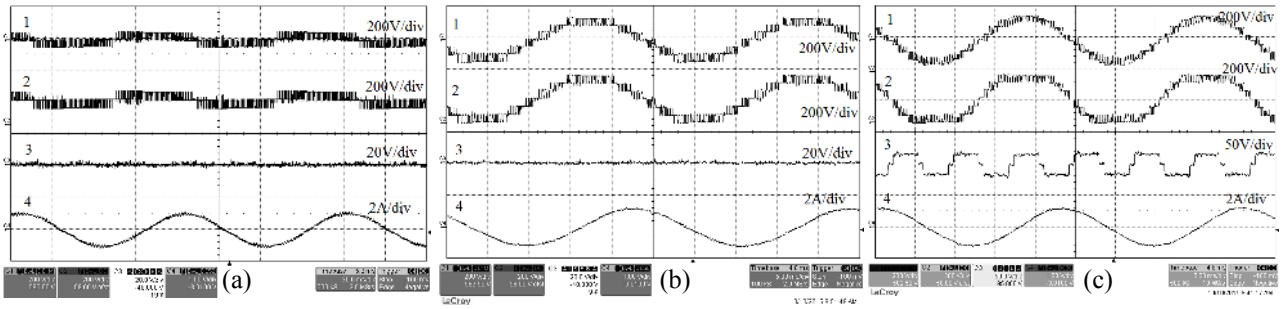


Fig. 11. Experimental results showing, 1) Motor Phase voltage (V_{an}), 2) Inverter pole voltage (V_{aO}), 3) Common mode voltage (V_{nO}), 4) Phase current (i_a). a) 10 Hz (m = 0.2) operation of inverter with zero CMV for phase 'a'. Time scale: 20ms/div. b) 40 Hz (m = 0.80) operation of inverter with zero CMV for phase 'a'. Time scale: 5ms/div. c) 45 Hz operation of inverter with reduced CMV $V_{dc}/18$ for phase 'a'. Time scale: 5ms/div.

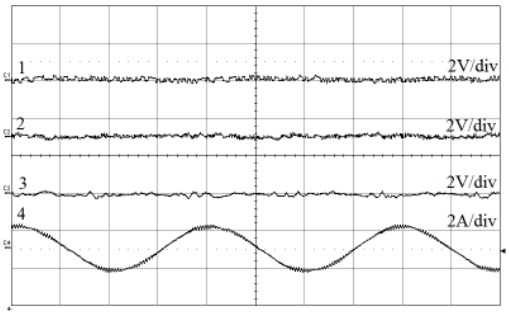


Fig. 12. Experimental results showing, 1) $V_{dc}/2$ capacitor voltage ripple (ΔV_ca1), 2) $V_{dc}/3$ capacitor voltage ripple ($\Delta V_{ca}2$), 3) $V_{dc}/6$ capacitor voltage ripple ($\Delta Vca3$), 4) phase current (i_a) for 10 Hz (m = 0.20) operation at no load. Time scale: 20ms/div.

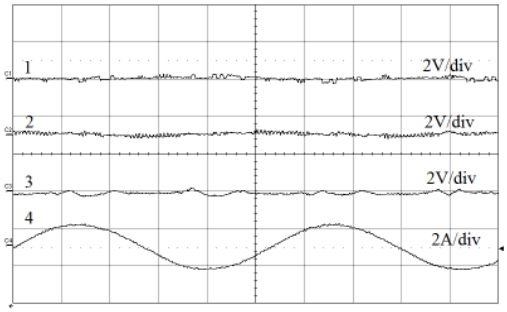


Fig. 13. Experimental results showing, 1) $V_{dc}/2$ capacitor voltage ripple ($\Delta Vca1$), 2) $V_{dc}/3$ capacitor voltage ripple ($\Delta Vca2$), 3) $V_{dc}/6$ capacitor voltage ripple ($\Delta Vca3$), 4) Phase current (i_a) for 40 Hz (m = 0.80) operation at no load. Time scale: 5ms/div.

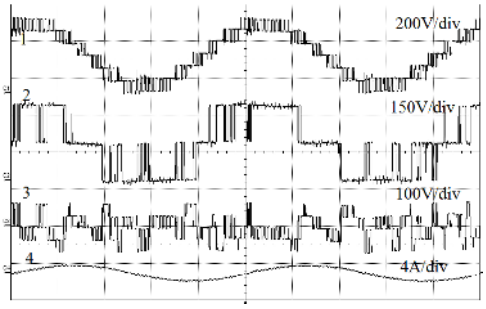


Fig. 14. Experimental results showing, 1) Inverter pole voltage (V_{aO}) , 2) INV-1 pole voltage ($V_{A'O}$, (Fig. 1)), 3) INV-2 pole voltage ($V_{aA'}$), 4) Phase current (i_a) for 40 Hz (m = 0.80) operation of inverter with zero CMV for phase 'a'. Time scale: 5ms/div.

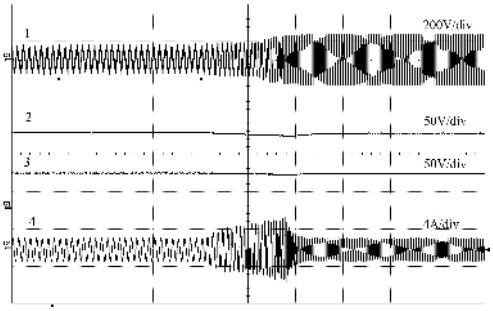


Fig. 15. Experimental results of sudden acceleration of motor from 15 Hz to 40 Hz in 1s. Waveforms shown are 1) motor phase voltage (V_{an}), 2) $V_{dc}/3$ capacitor voltage ($Vca2$), 3)$V_{dc}/6$ capacitor voltage ($Vca3$) and 4) Phase current (i_a). Time scale: 0.5 s/div.

open loop V/f control scheme. Synchronous PWM technique is used for testing the inverter topology. Number of samples per sector is taken as 12 for fundamental frequency ranging from 15 Hz to 25 Hz, 9 for 25 Hz to 37.5 Hz, and 6 for 37.5 Hz to 45 Hz. For fundamental frequency below 15 Hz inverter is operated with a constant switching frequency of 900 Hz. Simulation results under various operating conditions are presented. Fig. 7(a) and Fig. 8(a) shows the zero CMV steady state operation of inverter for fundamental frequencies 10 Hz and 40 Hz. Fig. 7(b), Fig. 7(c), Fig. 8(b) and Fig. 8(c) shows the performance of predictive capacitor voltage controller over a hysteresis band based capacitor voltage controller in terms of voltage ripple during no load and full load for fundamental frequencies 10 Hz and 40 Hz with same SVPWM technique. It can be seen that predictive controller gives better capacitor voltage control over hysteresis band based controller. Fig. 9(a) shows the reduced CMV steady state operation of inverter for a fundamental frequency of 45 Hz. Normal seven level inverter operation at 45 Hz is presented in Fig. 9(b) for comparing the CMV switching with the new SVPWM technique. Fig. 9(a1) and Fig. 9(b1) shows the frequency spectrum of inverter pole voltage V_{aO} for reduced CMV operation and normal seven level inverter operation. A 3 phase, 400V, 3.7kW, 50 Hz, 4 pole induction motor drive with open loop V/f control scheme is implemented in hardware for testing the proposed topology. TMS320F28335 DSP is used as the main controller and Xilinx SPARTAN-3 XC3S200 FPGA as the PWM signal generator with a dead time of 2.5 μs. The experimental set-up is shown in Fig. 10. The non-idealities present in the

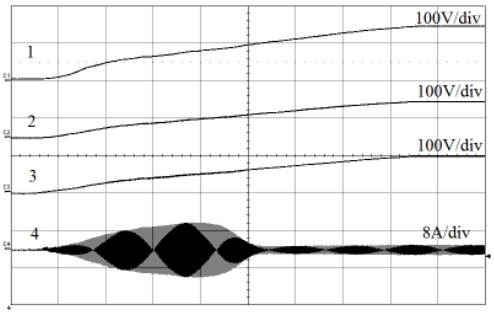


Fig. 16. Experimental results showing charging of capacitor voltages to the reference voltage from a relaxed state when inverter is switched on. Wave forms shown are 1) $V_{dc}/2$ capacitor voltage ($Vca1$) , 2) $V_{dc}/3$ capacitor voltage ($Vca2$) v, 3) $V_{dc}/6$ Capacitor voltage ($Vca3$), 4) Phase current (i_a) for phase 'a'. Time scale: 1s/div.

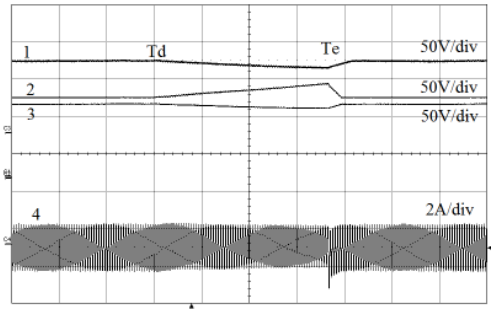


Fig. 17. Experimental results showing the ability of capacitor voltage controllers to bring back all the capacitors to the reference voltage. Wave forms shown are 1) $V_{dc}/2$ capacitor voltage ($Vca1$), 2) $V_{dc}/3$ capacitor voltage ($Vca2$), 3) $V_{dc}/6$ capacitor voltage ($Vca3$), 4) Phase current(i_a) for phase 'a'. Time scale: 0.5s/div.

experiment which are not considered during simulation are, on state voltage drop of switches, voltage drop due to capacitor ESR and dead time effects. The effect of these non-idealities in the inverter operation can be neglected with sufficiently high DC bus voltage with higher modulation indices. These non-idealities will be critical for operating frequency below 5 Hz, because the fundamental voltage will be comparable to the switch voltage drop. Because of this reason, the motor phase current gets distorted and need switch voltage drop compensation in the modulating signal. Experimental results showing the steady state operation of inverter with predictive control for fundamental frequencies 10 Hz and 40 Hz are presented in Fig. 11(a) and Fig. 11(b). Fig. 14 shows the pole voltages of INV-1 and INV-2 (Fig. 1) for 40Hz operation. We can see that INV-1 switches at a lower frequency compared to INV-2. Experimental results showing the capacitor voltage ripple with predictive control for 10 Hz and 40 Hz operation is shown in Fig. 12 and Fig. 13. From the results it can be seen that capacitor voltage ripple is very less (ΔV <0.5 V). Experimental results for reduced CMV operation of inverter is shown in Fig. 11(c) for a fundamental frequency of 45 Hz. Fig. 15 shows motor phase voltage (V_{an}), $V_{dc}/3$ capacitor voltage ($Vca2$), $V_{dc}/6$ capacitor voltage ($Vca2$) along with machine current (i_a) for an acceleration of motor from 15 Hz to 40 Hz in 1s. It can be seen that all the capacitor voltages are tightly controlled during this transient operation. Fig. 16 shows the capacitor voltage build-up when inverter is turned on with all capacitors in discharged condition. The ability of capacitor voltage controller to restore the capacitor voltage back to reference voltage is tested by disabling the controller at time T_d and enabling at T_e. Fig. 17 shows that the capacitor voltages deviates from reference voltages at T_d and quickly come back to the reference voltages when balancing algorithm is enabled at T_e.

VII. Conclusion

In this paper, a cascaded multilevel inverter topology with predictive capacitor voltage control is presented for SVPWM based zero and reduced CMV operation. Capacitor voltage control is based on minimizing the selected cost function for various redundant switching states. For every sampling instant, the capacitor voltages are predicted using previous capacitor voltages, load current and inverter switching function. Switching state which gives minimum value for the cost function is selected. This method helps in reducing the capacitor voltage ripple. For the cascaded inverter topology presented, cost function for each phases are evaluated separately to independently control capacitors of each phase. This approach reduces the number of computations required for MPC. Detailed simulation and experimental results are presented in this paper for various operating conditions with predictive capacitor voltage control. To extend the range of linear modulation and to improve the DC bus utilization of the inverter, a new SVPWM method with reduced CMV switching (CMV magnitude of $V_{dc}/18$ and CMV frequency of three times fundamental) is also proposed in this paper. Using this new technique 10% increase in linear modulation range is possible compared to zero CMV operation. The reduced CMV algorithm presented in this paper can be applied to any n-level (n is odd and n $\neq$ 3) inverter topology. The inverter topology and capacitor balancing is tested for zero CMV operation and reduced CMV operation and steady state and transient operation results are presented.

References

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron*, vol. 57, no. 8, pp. 2581–2596, Aug 2010.

[3] J. D. Barros, J. F. A. Silva, and . G. A. Jesus, "Fast-predictive optimal control of npc multilevel converters," *IEEE Trans. Ind. Electron*, vol. 60, no. 2, pp. 619–627, Feb 2013.

[4] J. Amini, "An effortless space-vector-based modulation for n -level flying capacitor multilevel inverter with capacitor voltage balancing capability," *IEEE Trans. Power Electron*, vol. 29, no. 11, pp. 6188–6195, Nov 2014.

[5] S. Thielemans, T. J. Vyncke, and J. Melkebeek, "Weight factor selection for model-based predictive control of a four-level flying-capacitor inverter," *IET Power Electronics*, vol. 5, no. 3, pp. 323–333, March 2012.

[6] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector pwm," *IEEE Trans. Power Delivery*, vol. 27, no. 3, pp. 1154–1161, July 2012.

[7] M. A. Perez, P. Cortes, and J. Rodriguez, "Predictive control algorithm technique for multilevel asymmetric cascaded h-bridge inverters," *IEEE Trans. Ind. Electron*, vol. 55, no. 12, pp. 4354–4361, Dec 2008.

[8] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded h-bridge inverters," *IEEE Trans. Ind. Electron*, vol. 57, no. 8, pp. 2691–2699, Aug 2010.
[9] T. Geyer and S. Mastellone, "Model predictive direct torque control of a five-level anpc converter drive system," *IEEE Trans. Ind. Appl*, vol. 48, no. 5, pp. 1565–1575, Sept 2012.
[10] P. R. Kumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A three-level common-mode voltage eliminated inverter with single dc supply using flying capacitor inverter and cascaded h-bridge," *IEEE Trans. Power Electron*, vol. 29, no. 3, pp. 1402–1409, March 2014.
[11] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron*, vol. 22, no. 5, pp. 1672–1681, Sept 2007.
[12] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron*, vol. 57, no. 7, pp. 2197–2206, July 2010.
[13] M. Saeedifard, P. M. Barbosa, and P. K. Steimer, "Operation and control of a hybrid seven-level converter," *IEEE Trans. Power Electron*, vol. 27, no. 2, pp. 652–660, Feb 2012.
[14] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," *IEEE Trans. Ind. Electron*, vol. 55, no. 12, pp. 4312–4324, Dec 2008.
[15] P. M. Sanchez, O. Machado, E. J. B. Pea, F. J. Rodrguez, and F. J. Meca, "Fpga-based implementation of a predictive current controller for power converters," *IEEE Trans. Ind. Info*, vol. 9, no. 3, pp. 1312–1321, Aug 2013.
[16] R. O. Ramirez, J. R. Espinoza, P. E. Melin, M. E. Reyes, E. E. Espinosa, C. Silva, and E. Maurelia, "Predictive controller for a three-phase/single-phase voltage source converter cell," *IEEE Trans. Ind. Info*, vol. 10, no. 3, pp. 1878–1889, Aug 2014.
[17] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive control of ac-ac modular multilevel converters," *IEEE Trans. Ind. Electron*, vol. 59, no. 7, pp. 2832–2839, July 2012.
[18] S. Chen, T. A. Lipo, and D. Fitzgerald, "Source of induction motor bearing currents caused by pwm inverters," *IEEE Trans. Energy Convers*, vol. 11, no. 1, pp. 25–32, Mar 1996.
[19] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, "Bearing currents and their relationship to pwm drives," *IEEE Trans. Power Electron*, vol. 12, no. 2, pp. 243–252, Mar 1997.
[20] M. Cacciato, S. Caro, G. Scarcella, G. Scelba, and A. Testa, "Improved space-vector modulation technique for common mode currents reduction," *IET Power Electronics*, vol. 6, no. 7, pp. 1248–1256, August 2013.
[21] P. P. Rajeevan and K. Gopakumar, "A hybrid five-level inverter with common-mode voltage elimination having single voltage source for im drive applications," *IEEE Trans. Ind. Appl*, vol. 48, no. 6, pp. 2037–2047, Nov 2012.
[22] S. K. Hoseini, J. Adabi, and A. Sheikholeslami, "Predictive modulation schemes to reduce common-mode voltage in three-phase inverters-fed ac drive systems," *IET Power Electronics*, vol. 7, no. 4, pp. 840–849, April 2014.
[23] P. Lezana, R. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Trans. Ind. Electron*, vol. 56, no. 6, pp. 1839–1846, June 2009.
[24] J. Leon, S. Kouro, L. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage source inverters in past, present and future power electronics," *IEEE Trans. Ind. Electron*, vol. PP, no. 99, pp. 1–1, 2016.
[25] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector pwm signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *IEE Proc. Electr. Power Appl*, vol. 152, no. 2, pp. 297–309, March 2005.

Arun Rahul S received the B.Tech degree in Electrical Engineering from the Rajiv Gandhi Institute of Technology, Kottayam, India, and the M.Tech degree in Machine Drives and Power Electronics from Indian Institute of Technology, Kharagpur, India. He is currently working towards the Ph.D. degree in the Department of Electronic Systems Engineering(formerly CEDT), Indian Institute of Science, Bangalore. His research interests include multilevel power converters, motor drives, power converters for renewable energy conversion and power quality.

R. Sudharshan Kaarthik (S'10) received the B.Tech degree from National Institute of Technology, Rourkela, India in 2010 and the M.Tech degree and PhD. degree from Department of Electronic Systems Engineering(formerly CEDT), Indian Institute of Science, Bangalore, India in 2012 and 2015 respectively. He is currently working in Concordia University, Canada. His research interests are in the areas of PWM converters and motor drives.

K. Gopakumar (M'94-SM'96-F'11) received the B.E., M.Sc. (Engg.), and Ph.D. degrees from the Indian Institute of Science, Bangalore, India, in 1980, 1984, and 1994, respectively. He was with the Indian Space Research Organization, Bangalore, India from 1984 to 1987. He currently holds the position of professor at the Department of Electronics System Engineering (formerly Center for Electronics Design and Technology), Indian Institute of Science. Dr. Gopakumar is a Fellow of IEEE, Institution of Electrical and Telecommunication Engineers India and Indian National Academy of Engineers. He is currently a Co-Editor in Chief of IEEE Transaction on Industrial Electronics and also a Distinguished Lecturer of IEEE Industrial Electronics Society(IES). His research interests include PWM converters and high power drives.

Leopoldo G. Franquelo (M'84-SM'96-F'05) received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Seville (US), Seville, Spain, in 1977 and 1980, respectively. He is currently with the Department of Electronics Engineering, US. His current research interests include modulation techniques for multilevel inverters and applications to power electronic systems for renewable energy systems. Dr. Franquelo has been a Distinguished Lecturer since 2006, an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 2007, and Co-Editor-in-Chief since 2014. He was a Member-at-Large of the IES AdCom (2002-2003), the Vice President for Conferences (2004-2007), and the President Elect of the IES (2008-2009). He was the President of the IEEE Industrial Electronics Society (2010-2011).

Jose I. Leon (S'04-M'07-SM'14) was born in Cadiz, Spain, in 1976. He received the B.S., M.S., and Ph.D. degrees in telecommunications engineering from the University of Seville (US), Seville, Spain, in 1999, 2001, and 2006, respectively. He is currently an Associate Professor with the Department of Electronic Engineering, US. His research interests include electronic power systems, modulation and control of power converters, and renewable energy systems. Dr. Leon was a recipient (as coauthor) of the 2008 Best Paper Award of the IEEE Industrial Electronics Magazine and the 2012 Best Paper Award of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. He was the recipient of the 2014 IEEE Industrial Electronics Society Early Career Award and is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.