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Negative capacitance in optically sensitive metal-insulator-semiconductor-metal structures

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We report a strong negative capacitance effect in back to back combination of a metal-insulator-semiconductor (MIS) structure and a metal-semiconductor junction, which is fabricated on an n type Silicon-on-Insulator substrate. The MIS capacitor comprises a SiO_2-HfO_2 insulator stack with embedded Pt nanoparticles. The capacitor undergoes a voltage stress process and thereby turns into a varactor and a photodetector. The negative capacitance is observed only under illumination in structures that employ a Schottky back contact. A symmetric double or an asymmetric single negative capacitance peak is observed depending on the nature of illumination. The phenomenon is attributed to the modulation of the semiconductor conductance due to photo generated carriers and their incorporation in trapping/de-trapping processes on interfacial and post filamentation induced defects in the insulator stack. The frequency range of the observed effect is limited to 100 kHz. Large ratios of light to dark and maximum to minimum of negative capacitances as well as of the obtained sensitivity to the applied voltage are, respectively, 105, more than 100, and 10-15. These were measured at 10 kHz under illumination at 365 nm with a power of 2.5×10^{-6} W. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4971401]

INTRODUCTION

Single metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) structures with Schottky type electrodes and back-to-back connected double MS (MSM) and MS-MIS (MISM) diodes comprise most high sensitivity, low noise photodetectors.[1] Their large photosensitivity is provided by an effective collection of photo generated minority carriers in the inter electrode area[2–4] due to an enhancement of the electric field at the electrode edges. The edge electric fields can be enhanced by pairs of junctions which are formed due to: (i) Electrodes with asymmetric barrier heights, for example, Schottky and Ohmic contacts or placement of an insulator layer under one of the electrodes, while the second is either an Ohmic or a Schottky type contact. (ii) Using electrodes with different areas or perimeters. (iii) Using unequal electrode areas and inter electrode spaces.[4] The enhanced electric field around electrodes deepens the depletion region in the semiconductor under the reverse biased electrode. Similar structures can be effectively used as varactors in which the capacitance is varied not only by voltage but also by the illumination intensity.[5,6]

MS and MIS structures are usually considered to be unipolar, and their capacitance is positive at any frequency.[1] However, under some specific conditions, the C-V characteristics of these structures exhibit both positive and negative capacitance branches when measured at low frequencies.[7–13]

The phenomenon of negative capacitance was previously observed in various structures and under different operating conditions. Several explanations were given for this peculiar phenomenon. Reference 10 discussed negative capacitance in Schottky diodes and MIS structures. Since the negative capacitance reduces with increasing frequency, it was concluded that it results from internal properties rather than from a parasitic series inductance. An alternative approach suggests[10,13–15] that an AC transient current leads to the measured negative capacitance. This occurs when the conductivity is inertial and the reactive current component is larger than the displacement current. The inertial conductivity is caused by interfacial charge trapping/de-trapping or by minority carrier generation-recombination processes. In other words, part of the generated carriers in the depletion region and of carriers injected from the electrodes are trapped by interfacial states. At specific frequencies and applied bias levels, carriers escape from trap states and contribute to the total current. However, they are delayed and hence a transient current is formed.

The formation of negative capacitance at different frequencies due to interfacial states in Schottky diodes was detailed in Ref. 16. Experiments on MSM diodes[7–9] revealed that emergence of negative capacitance requires either an asymmetric electrode structure (one rectifying and one Ohmic contact) or two Schottky contacts. The capacitance becomes negative due to a variation of the minority carrier density (injected from the forward biased electrode) in the neutral semiconductor region of the semiconductor, and this is strongly dependent on the barrier height of electrodes and the doping level of the semiconductor.[7,17] The reduction of minority carrier density as the frequency increases reduces the magnitude of the negative capacitance due to the limited life time of injected or generated carriers, which cannot follow the AC drive signal. Another possible explanation was suggested in Ref. 8 where it was claimed that the negative capacitance resulted from a loss of the Schottky contact–semiconductor interface charges at occupied states below the Fermi level due to impact ionization. A single negative capacitance peak in MIS structures with ultrathin SiO_2

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insulators was interpreted[11] to be a result of the local recombination in pinhole defects of majority (injected from the reverse biased electrode) and minority carriers (generated in the depletion region of the semiconductor). A detailed study of the influence of the interfacial SiO_2 thicknesses[11] concluded that the negative capacitance increases when the oxide layer includes pinholes,[18] which are a source of trap states. Moreover, the thin insulator makes possible direct tunneling of carriers. The role of illumination in the formation of the single negative capacitance peak was discussed in Ref. 12, where the observed phenomenon was attributed to local hole-electron recombination on laterally non-uniform ultra-thin oxide films, which enhance minority carrier photo generation in the depletion region.

In this paper, we report MISM structures, which show strongly enhanced, by illumination, negative capacitance and conductance peaks. We show that the voltage level for which the negative capacitance or conductance peak is obtained depends on the electrode properties and the light spot position relative to the electrodes.

EXPERIMENTAL PROCEDURE

The planar MSIM structures are similar to those described in Ref. 6. They were fabricated on a SOI substrate with a 2.9 μm thick phosphorous doped n-Si device layer having a resistivity of 90 Ohm cm. A 3 nm thermal SiO_2 tunneling layer followed by a 20 nm HfO_2 film with embedded Pt nanoparticles (NP) between the two dielectric layers make up the insulator stack. The Pt NPs were fabricated at low temperature[19,20] in the atomic layer deposition (ALD) system, in-situ with the HfO_2 layer similar to Ref. 6. A Pt film with an approximate thickness of 3 nm was deposited on top of the thermal SiO_2 layer using (Trimethyl)methylcyclopentadienylPlatinum (IV) (MeCpPtMe3) in an oxygen environment and at a substrate temperature of about 300 °C. The thin Pt film cannot maintain a homogeneous form and breaks forming of individual particles separated from each other. In contrast to Ref. 6, both electrodes include a Pd/Pt/Au stack (deposited by electron beam gun evaporation at room temperature) in order to form a high potential barrier. The gate (MIS part) and back (MS part) electrode areas were 1.75×10^{-6} cm^2 and 3.8×10^{-6} cm^2, respectively. A schematic illustration of two adjacent devices is shown in Fig. 1.

The inner electrode distance of all diodes was 5 μm. They were tested either as single devices or in a configuration where the gate and back contacts were of two separate, adjacent devices. In this case, the electrodes are connected via the silicon device layer and the inter electrode distance increased to 135 μm. The current-voltage (I-V), capacitance-voltage (C-V), and conductance-voltage (G-V) characteristics were measured at room temperature in three regimes of illumination. The first uses uniform illumination of the optical area of both branches of a single MISM structure. In the second case, the MIS part was illuminated and the MS section was dark and in the third, the MIS part was dark while the MS branch was under illumination. The latter two cases employed two adjacent diodes with the large inter electrode distance (135 μm).

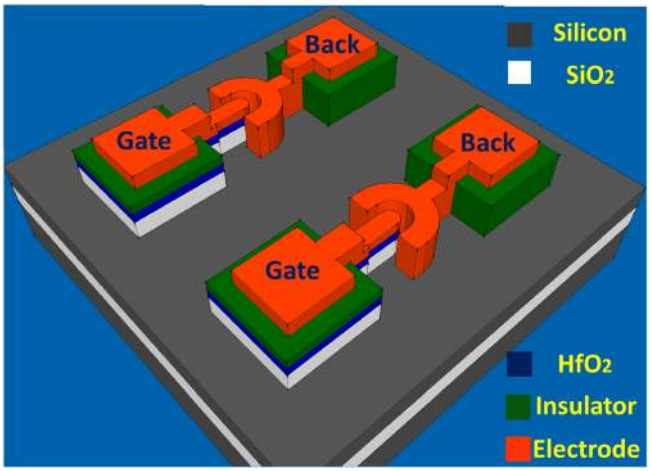

FIG. 1. Schematic description of two adjacent MISM structures.

The MISM structure underwent a voltage stress process[21] in order to form filament paths, which enable the leakage current flow. All tests were conducted for a variable gate voltage and a grounded back electrode. The I-V characteristics were measured using an Agilent 4155C Semiconductor parameter analyzer. The C_{pm}-V and G_{pm}-V characteristics were obtained from an HP4192A LF impedance analyzer operating in the parallel mode. Collimated illumination at 365 nm wavelength from a light emitting diode was coupled to the device under test via a lensed fiber. The corresponding illumination spot area for the fiber lens was roughly 1.7×10^{-6} cm^2, while the optical window area in all the structures was 1.8×10^{-6} cm^2.

Simple equivalent circuits of single MIS and MS Schottky capacitors are given in Figs. 2(a) and 2(b). Fig. 2(c) describes the equivalent circuits of a MIS and a Schottky MS diode connected in series and biased in opposite polarities. C_{ox} is the capacitance of the gate insulator in the accumulation regime; C_s is the capacitance induced by the voltage dependent depletion region in the semiconductor, which is connected in series with C_{ox} in an MIS structure; finally, capacitance C_{it} is induced by interfacial traps; G_{p1} and G_{p2} are the equivalent parallel conductance. C_{t1} and C_{t2} in the schematic circuit shown in Fig. 2(c) represent the total capacitances of all sub capacitors in Figs. 2(a) and 2(b), in

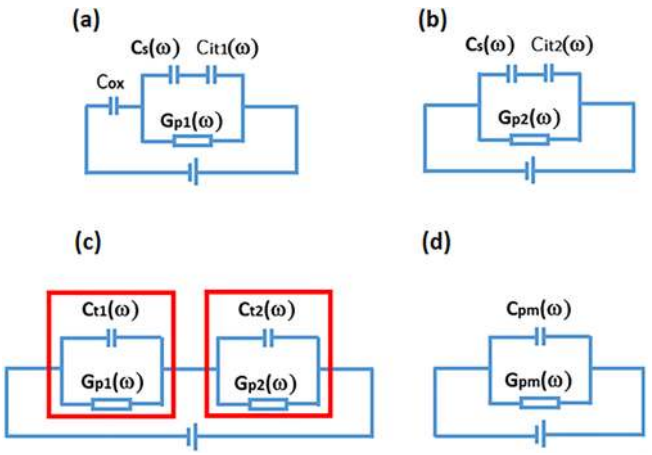

FIG. 2. Equivalent circuit diagrams of (a) MIS, (b) MS, (c) a MISM configuration, and (d) simplified measurement circuit of an MISM structure.

sections MIS and MS. C_{t1} and C_{t2}, respectively, are expressed by equations: $\frac{1}{C_{t1}} = \frac{1}{C_{ox}} + \frac{1}{C_s} + \frac{1}{C_{it1}}$ and $\frac{1}{C_{t2}} = \frac{1}{C_s} + \frac{1}{C_{it2}}$. Fig. 2(d) illustrates the simplified measurement circuit, which reflects an equivalent parallel total capacitance (C_{pm}) and a parallel conductance (G_{pm}) modulated at angular frequency $\omega = 2\pi f$, where f is the frequency of the applied AC signal.

EXPERIMENTAL RESULTS

Two sets of C_{pm}–V characteristics of a single MISM structure are shown in Fig. 3. Fig. 3(a) describes illumination dependent capacitance, measured at 10 kHz, while the capacitance changes with frequency under a constant illumination intensity of 2.5×10^{-6} W are shown in Fig. 3(b). Both junctions exhibit a bias and frequency independent capacitance of 20–30 fF in the dark. However, under uniform illumination, a clear transition to the negative capacitance regime is observed. The peak levels, which are strongly dependent on illumination and frequency, are obtained at bias levels of −1.1 V and +0.8 V. The insets in Figs. 3(a) and 3(b) show the evolution of the peak negative capacitance with illumination and frequency. At 2.5×10^{-6} W, the capacitance increases by a factor of 105 and 90, respectively, for the peaks marked I and II, compared to the dark while the capacitance ratio at 5 kHz compared to 100 kHz under an illumination of 2.5×10^{-6} W increases by a factor of 70 and 46, respectively. Under maximum illumination at 5 kHz, the voltage sensitivity of the negative part of the capacitance, $S = \frac{d \ln C}{d \ln V}$, is 13.

The capacitance level in the valley between the peaks is positive. Its value at zero bias is below 0.1 pF for all illumination intensities and frequencies. At large negative and positive bias levels, the capacitance is positive exhibiting a dependence on illumination and frequency common to depletion regions. The saturation capacitance due to inversion of the semiconductor surface by minority carriers is obtained at 2–2.5×10^{-6} W and 10 kHz.

The effective dielectric constant of the insulator stack determined in the inversion regime is 12.5, similar to that estimated from the accumulation capacitance in similar but unstressed structures.[21] Illumination at 2.5×10^{-6} W causes a significant increase in the effective dielectric constant (extracted from the absolute values of peak I in Fig. 3b, measured at f = 5 kHz), which reaches a value of 53.

A pair of peaks are also revealed on the (G_{pm}/ω) versus V characteristics shown in Fig. 4. These peaks vary with illumination and frequency in the same manner as the capacitance

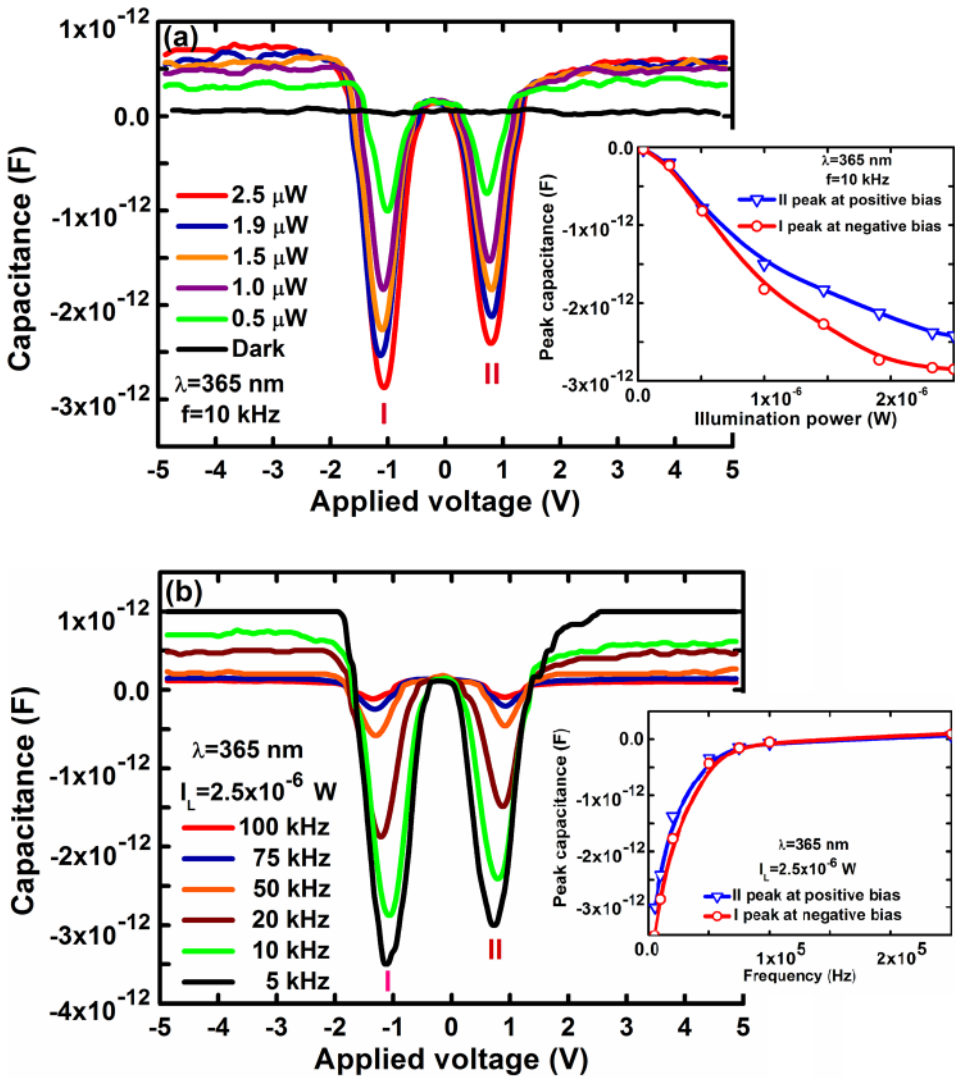

FIG. 3. C_{pm}-V characteristics of a MISM structure measured (a) at different illumination powers and a constant frequency. (b) Different modulation frequencies and a constant illumination power. Insets in (a) and (b) denote, respectively, illumination power and frequency dependencies of the peak I and II capacitances.

peaks shown in Fig. 3. The conductance varies linearly with illumination at any voltage near either peak, as shown in the inset to Fig. 4. These dependencies resemble static photodetector characteristics.

A different configuration we tested comprises a pair of MIS and MS diodes connected in a back-to-back configuration. The configuration employed one contact from each of two adjacent diodes which are placed sufficiently far from each other (135 μm) to enable illumination of one diode only. Figs. 5 and 6 describe measured C_{pm}–V and (G_{pm}/ω)-V characteristics when the gate (Fig. 5) or back electrode (Fig. 6) was illuminated. The applied voltage polarity, and therefore sweep directions, of the C_{pm}–V and (G_{pm}/ω)-V curves is related once more to the gate electrode.

The C_{pm}–V and (G_{pm}/ω)-V curves have only one peak in these cases; it appears at a bias level which is determined by which junction is illuminated. Interestingly, the peak values and the bias are the same as those obtained when the two junctions were illuminated simultaneously. At the same time, the capacitance of the dark diode is constant.

The total capacitance of the system (in accordance with the schematic circuit in Fig. 2(c) and the equation for $(1/C_{t1})$ at negative gate bias (see Fig. 5(a)) is determined by the depletion region and the interfacial state charging process due to photo generated minority carriers, while the reciprocal value $(1/C_{t2})$ of the large capacitance of the forward biased back electrode-semiconductor junction, including the accumulation region and interfacial traps, can be neglected. For a positive gate bias, the capacitance of the depletion layer of the dark reverse biased MS junction determines the total capacitance due to the large C_{t1} of the gate junction $(1/C_{t1} < 1/C_{t2})$. The depletion capacitance also limits the voltage range where the negative capacitance occurs to low bias levels near zero. This can be easily understood with help of the schematic circuit of an MIS structure which includes a series connection of the insulator and depletion capacitances and the series resistance of the contact and the semiconductor. The $(G_{pm}/\omega))$-V characteristics change with illumination in a similar manner (see Fig. 5(b)). Additionally, the behavior of the C_{pm}–V and (G_{pm}/ω)-V characteristics when the MS branch is illuminated and the MIS part is dark is similar (see Fig. 6). Thus, we conclude that the two symmetric peaks observed under uniform illumination of both diodes result from contributions of capacitance changes with voltage of each junction which is reverse biased.

DISCUSSION

A survey of the literature and our experimental data indicate that two main reasons cause negative capacitance in MISM structures. They are nonlinear modulation of the

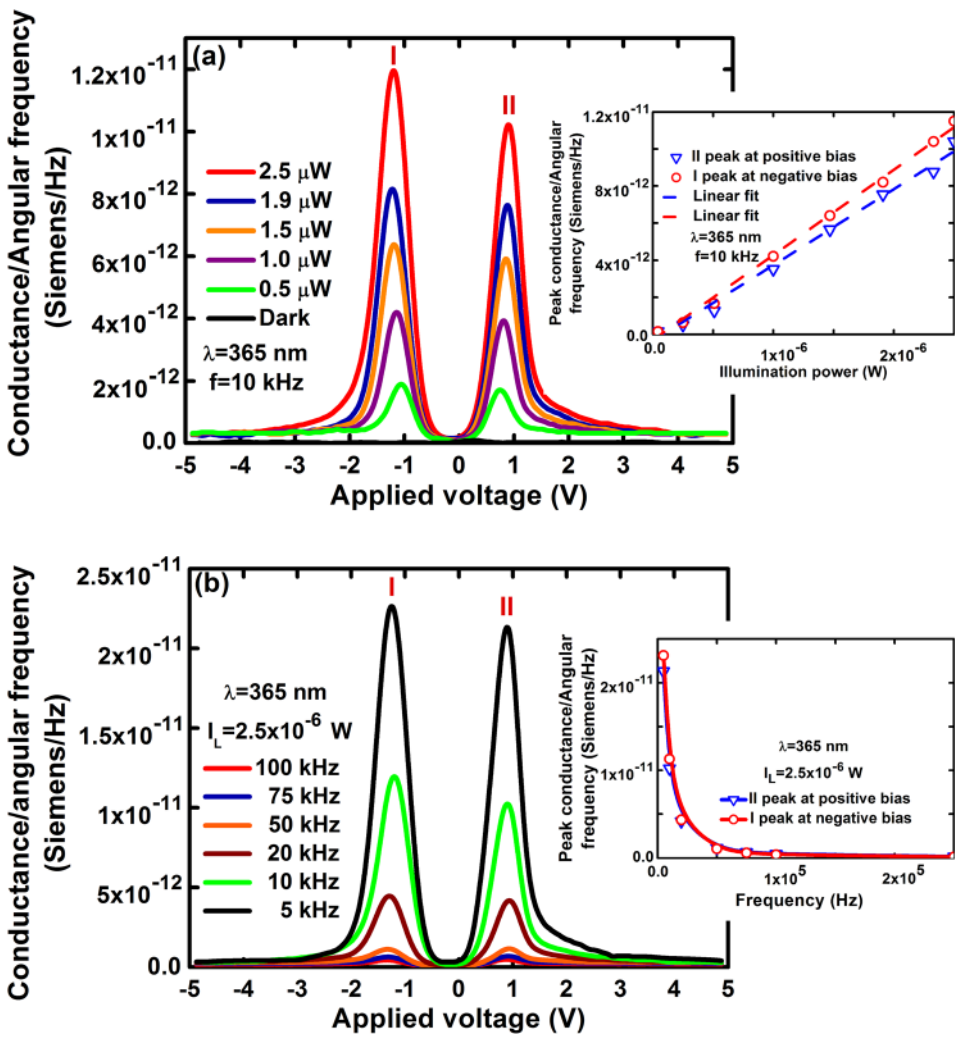

FIG. 4. (G_{pm}/ω)-V characteristics of a MISM structure measured (a) at different illumination powers and a constant frequency. (b) Different modulation frequencies and a constant illumination power. Insets in (a) and (b) denote, respectively, illumination power and frequency dependencies of the peak I and II conductance. In the inset of (a), the dashed lines are a liner fit.

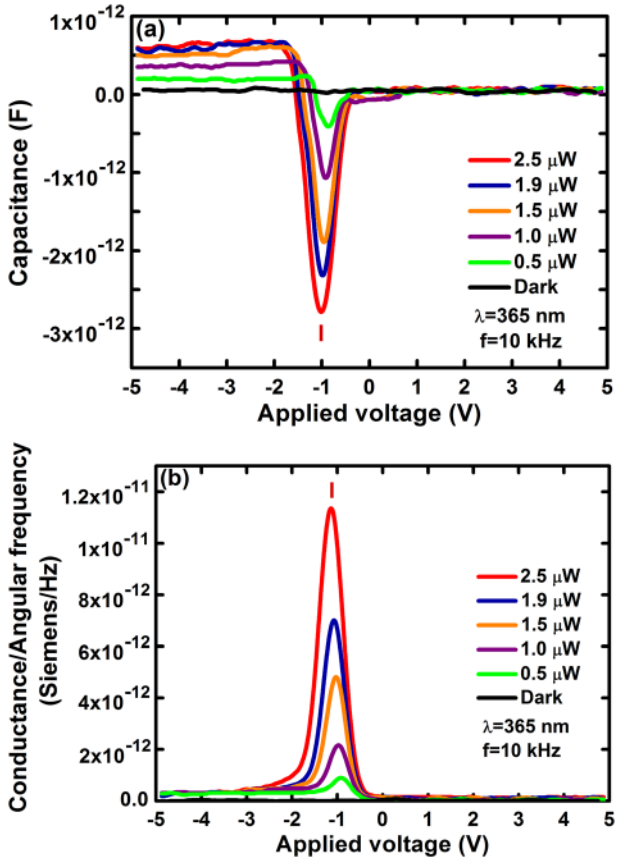

FIG. 5. (a) C_{pm}-V and (b) (G_{pm}/ω)-V characteristics of a MISM structure measured (a) at different illumination powers and a constant frequency. The gate electrode is illuminated, while the back electrode is dark.

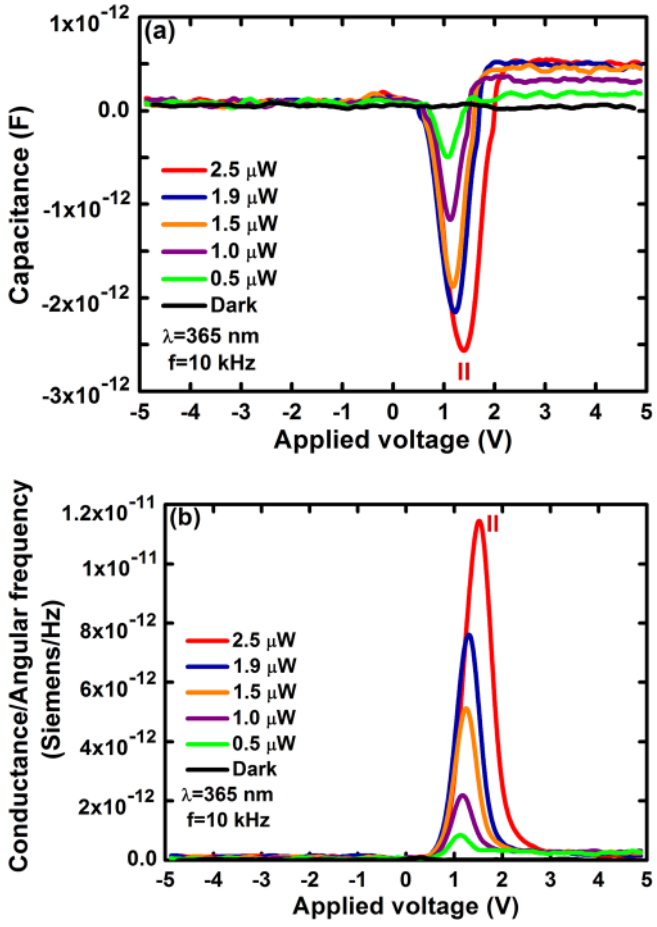

FIG. 6. (a) C_{pm}-V and (b) (G_{pm}/ω)-V characteristics of a MISM structure measured (a) at different illumination powers and a constant frequency. The gate electrode is dark, while the back electrode is illuminated.

neutral part of the semiconductor and/or trapping and detrapping at interfacial states caused by a variation of the minority carrier density.

The effects of traps in the HfO_2 layer due to oxygen vacancies, as well as at the boundaries between the insulator and the Pt NCs, on dynamical characteristics and on leakage current of non-volatile memory capacitors were discussed in Ref. 22. The oxygen vacancies result from breaking of Hf-O chemical bonds.[23,24] Moreover, when the HfO_2 layer is grown on top of the NPs, the initial atomic layers covering the NPs grow as a porous rather than a continuous film,[25,26] with a large stoichiometric deficiency of oxygen. Details of the different charge states for oxygen vacancies in monoclinic HfO_2 were detailed in Refs. 27 and 28. Another reason of induced traps and their penetration to the interface of semiconductor is the filament paths induced by voltage stress as described in Ref. 21. These paths are used as channels of photocurrent by photo generated minority carriers induced in the depletion layer and their movement from the inversion layer at the semiconductor interface to the gate electrode.[21]

The energy distribution of the interface trap density (D_{it}) along their position in the Si band gap was established by the conductance method,[29] which uses a plot of the equivalent parallel conductance normalized to angular frequency G_p/ω versus frequency at constant applied voltages. First, G_p/ω is calculated from measured C_{pm} and G_{pm}. Second, the maximum of G_p/ω-f dependence and consequent values of the resonant frequencies are extracted, which allows the calculation of the D_{it} and the establishment of the characteristic time, which is related to the peak of the angular frequency through $\tau_{it} \sim 1/\omega$. Here, τ_{it} denotes the time needed for excitation of the captured carriers from trap states located at energy $\Delta E = E_B - E_t$. E_B and E_t are, respectively, the energy of the majority carriers band edge and the energy depth of the interfacial trap states in the vicinity of the semiconductor band gap. In accordance with the Shockley Read Hall statistics,[30–32] ΔE is related to the traps and semiconductor parameters by $\Delta E = kT \ln(\tau_{it}\sigma\upsilon_{th}N_c)$, where σ, υ_{th}, and N_c, respectively, are the trap cross section, thermal velocity of the free carriers, and effective density of states of the majority carrier band. Interfacial states density is calculated from the peaks $(G_p/\omega)_{\max}$ of G_p/ω-f dependences (achieved at $\omega\tau_{it} \sim 1.98$ in the case of the continuum distribution of the traps) by $D_{it} = 2.5/Aq(G_p/\omega)_{max}$,[33] where A and q, respectively, are the gate electrode area and elementary charge. The following values $\sigma = 2.5 \times 10^{-15}\text{cm}^2$, $\upsilon_{th} = 1.5 \times 10^7$ cm/s, and $N_c = 2.8 \times 10^{19}$ cm^{-3} (Refs. 1 and 34) and experimental τ_{it} were used for the calculation of ΔE and D_{it}.

The symmetric distribution of the D_{it} between 0.37 and 0.43 eV was revealed in the range of observed negative capacitance peaks. The resultant extracted values of the D_{it} changed insignificantly from 2×10^{12} cm^{-2}eV^{-1} to

$2.5 \times 10^{12}\,cm^{-2}eV^{-1}$ in the vicinity of 0.37–0.41 eV and then sharply increase to about 1.7×10^{13} $cm^{-2}eV^{-1}$. The estimated energy range is close to 0.35 eV and 0.5 eV, mentioned in Ref. 28 as oxygen vacancies, and traps the energy depth of about 0.48 eV with a density of 7.1×10^{12} cm^{-2} extracted in Ref. 21. In accordance with Refs. 21 and 28, we suppose that the traps, the parameters of which were estimated above, can be identified as negative oxygen vacancies originating from defects inside the HfO_2 layer and at the defective boundary of Pt NCs and covering HfO_2 sublayers, redistributed into the filament channels.

A negative gate bias enhances the migration of oxygen vacancies across the HfO_2 film toward the Si, while minority carriers (holes), whose density depends (at a constant frequency) on illumination intensity, are accumulated at the semiconductor surface. Some of these are trapped by negatively charged oxygen vacancies and partially neutralize the traps. This reduces, in turn, the capacitance. The capacitance rises after reaching a maximum absolute value, due to the increase of negatively charged oxygen vacancies with the rising bias. The C_{pm}–V curve passes through zero and then depends only weakly on the reverse bias voltage, similar to the behavior of MIS structures in the depletion regime. The saturated capacitance value is determined by the series combination of the depletion and insulator stack capacitances. An increase of the illumination intensity and a reduction of the operational frequency determine the generated minority carrier density and therefore the traps' charging/discharging level and thus the negative capacitance magnitude.

The negative capacitance can originate also from a nonlinear modulation of the semiconductor neutral part by a variation of the minority carrier density. The conductance modulation is caused by penetration of minority carriers that drift from the positive biased back electrode toward the reverse biased gate electrode. The modification of neutrality is compensated for by majority carriers that are injected from the negatively biased electrodes and drift towards the back electrode. Some of these majority carriers recombine with interfacial states, filled by the trapped minority carriers, and re-localize them. These add to a transient current which lags behind the DC current. Another part of the majority carriers contributes to the re-establishment of neutrality close to the reverse biased electrode. Hence, a modulation of the conductance of the semiconductor bulk takes place in this local region, which yields the negative capacitance.

These processes depend on the minority carrier ability to follow the AC drive frequency. Changes due to illumination of the minority carrier density in the depletion region and the neutral part of the bulk of semiconductor intensify both the conductance modulation and the interfacial states charging/discharging and hence the appearance negative capacitance. The presence of interfacial states alone does not guaranty the existence of negative capacitance; it is imperative to also consider the electrodes' properties since those are the sources of free carriers injected into the semiconductor and hence of the conductance modulation. In the case of an asymmetric electrode configuration, induced by dissimilar barrier heights (caused by different electrode materials or by interfacial dielectric stacks under one electrode), the distribution of the electric field in the lateral and vertical directions changes significantly the small signal response of minority carriers in the inter electrodes neutral and in the depletion regions which enhances the negative capacitance.

The negative capacitance occurs in MIS or MS structures with contacts that avail large Schottky barriers and which include large interfacial state densities under reverse bias.[7,9] Additionally, illumination enhances the magnitude of the negative capacitance peaks. The effect of illumination on the barrier height results from carrier injection into the neutral and depletion regions of the semiconductor and can be quantified by measurements and an analysis of the I-V characteristics.

Fig. 7 shows a typical set of I-V curves measured for the MISM structure in two illumination regimes, analogous to the voltage dependent capacitance and conductance characteristics. For the single (5 μm inter electrode distance) structure, the illumination is uniform while for the two adjacent diode configuration, the back electrode was in the dark. Fig. 7(a) refers to the uniform illumination where the I-V curves are almost symmetric with respect to the bias polarity. In contrast, when the back electrode is dark, the characteristics are vastly asymmetric as seen in Fig. 7(b). The inset of Fig. 7(a) shows the static conductance dependence on voltage (extracted from the I-V curves). The obtained behavior is the same as the corresponding AC conductance shown in Fig. 4(a). The inset in Fig. 7(b) is a zoomed view of the positive bias portion of the curve. The dependencies on illumination power of the photocurrent measured at a bias of ± 5 V are shown in Figs. 7(c) and 7(d). The linear character of the curves in Figs. 7(c) and 7(d) resembles the dependence of the conductance on illumination power (shown in Fig. 4). The change in leakage current with illumination under positive bias even when the back electrode is dark (see inset in Fig. 7(b)) is attributed to the well-known side illumination effect which in Si is noticeable around 100–150 μm from the illuminated point.[35] This fact is clearly demonstrated in the I-V curves (see Figs. 7(b) and 7(d)), where the photocurrent at a reverse biased back electrode is indeed smaller than that for an illuminated gate area under similar bias conditions but is almost two orders of magnitude larger than that when the entire structure is dark.

The effect of illumination on the Schottky barrier height and therefore on the photo sensitivity was considered in Refs. 4 and 36–39. The reduction of the Schottky barrier height in nanowire photo detectors was found to be[37] due to an illumination induced variation of the quasi Fermi level relative to equilibrium, this in addition to the well-known lowering by the image force potential. MOS structures containing porous islands where MS junctions are formed were addressed in Ref. 38. Under illumination, photo generated holes accumulate at the Si surface along the perimeter of the islands, and this enhances the electric field around specific local points, thereby lowering the Schottky barrier height. Another mechanism was suggested in Ref. 4 and 39, where an enhancement of the photocurrent in MOS structures comprising SiO_2 or SiO_2/HfO_2 tunneling layers was explained by

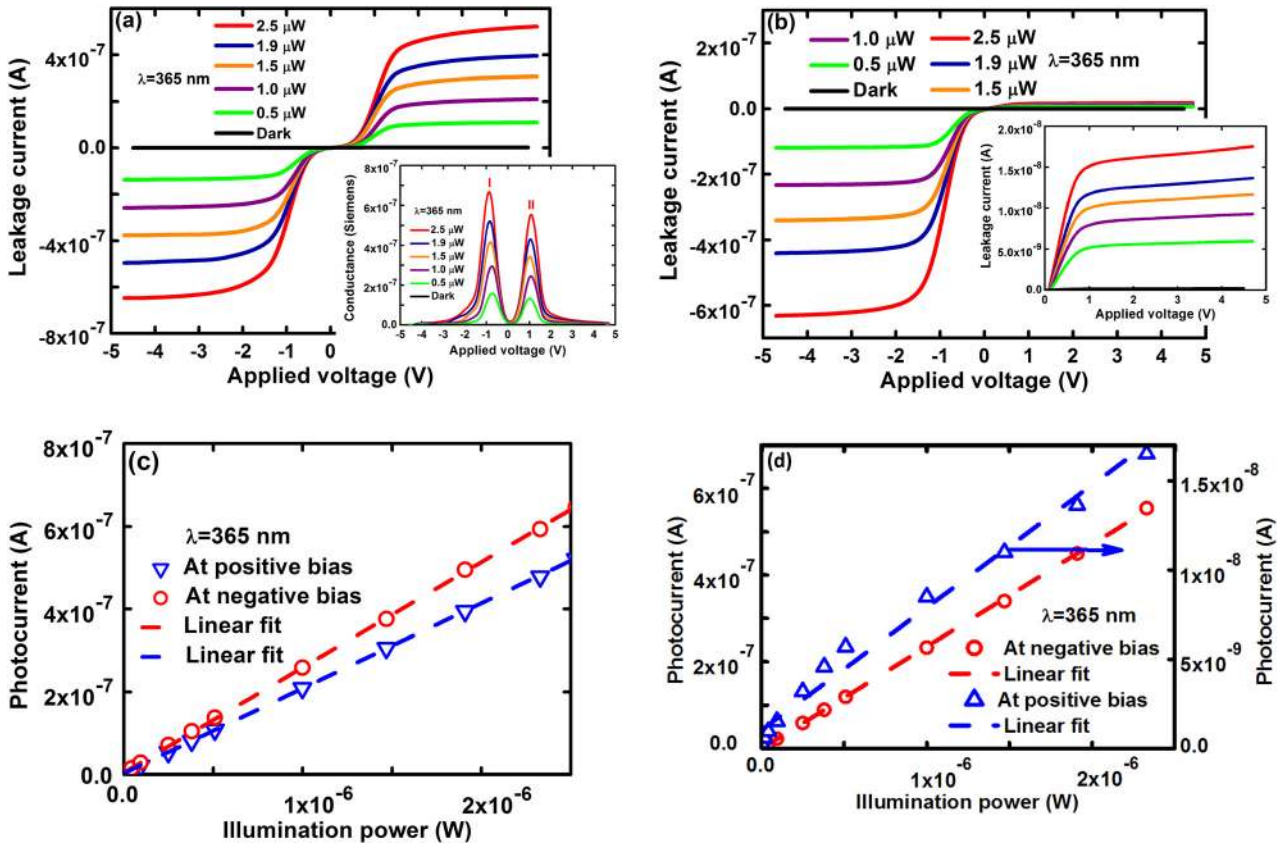

FIG. 7. I-V characteristics of a MISM structure at (a) uniform illumination. (b) The gate area only is illuminated, while the back electrode is dark. Insets in (a) and (b) illustrate, respectively, static conductance-voltage dependence and a zoomed view of the I-V characteristics at positive gate bias. (c) and (d) Photocurrent versus illumination power characteristics, for uniform illumination and when the gate area only is illuminated, respectively. The distances between gate and back electrodes in (a) and (c) are 5 μm; in (b) and (d) 135 μm. Dashed lines are a linear fit.

an enhanced edge effect. Deep depletion absorption in the Si layer near the Schottky electrode increases, in those diodes, the edge fringing field effect.

We extracted the zero bias barrier height from the measured I-V characteristics using the method described in Refs. 40 and 41. Figs. 8(a) and 8(d) show the results for the symmetric and asymmetric cases, respectively. Two facts were revealed: (i) the dark barrier height at the gate (0.705 eV) is larger than at the back electrode (0.63–0.64 eV) and (ii) the effect of illumination power is different for the two structures. The light to dark barrier height ratio is about 1.52 for the gate electrode in both cases and 1.32 and 1.2 for the back electrodes, respectively, for the short and large inter electrode distance configurations. This difference is the cause of the slight asymmetric I–V characteristics in the uniform illumination case. The influence of the barrier heights on the asymmetric behavior of the negative capacitance peak is clearer in the case where only one junction is illuminated (see Fig. 5 or 6). The barrier height reduction of the back electrode with illumination (even though it is dark) is due to diffusion of photo generated minority carriers via the Si layer, from the illuminated gate area ɪ to the depletion layer of the reverse biased diode.[35] A second reason is drift under applied electric field of minority carriers.[42] Minority carriers that accumulate at the interface attract majority carriers from the reverse biased electrode and hence cause a reduction of the effective barrier height.[43]

CONCLUSION

To conclude, we have demonstrated photosensitive back to back connected MIS-MS planar structures with Pt NPs, fabricated at low temperatures by ALD, embedded between HfO_2 and a thermal SiO_2 tunneling oxide, fabricated on a SOI substrate. Filament type leakage paths induced by voltage stress of the MIS part transform the nonvolatile memory device[6] to a varactor and a photodetector. The addition of asymmetric electrodes yields negative capacitance peaks, which are sensitive to illumination and frequency. Illumination of the entire structure or illumination of one half only controls the nature of the negative capacitance function where an almost symmetric double peaked or a single peak character can be obtained. The maximum light to dark ratio of the capacitance peaks is more than one hundred, while the sensitivity to voltage S under maximum illumination and at 5 kHz is 13. The maximum frequency where a negative capacitance is obtainable is 100 kHz. The dependencies of the conductance-voltage curves on illumination intensity and frequency are identical to the capacitance-voltage and current-voltage characteristics. The dependence of the conductance and capacitance on frequency stems from the limited ability of minority carriers to follow to AC signal, which leads to a transient current.[44] The results reported here differ from those in Refs. 7–9 where prior to the capacitance drops to below zero, a positive capacitance peak is observed. Also the data in Refs. 11 and 12 exhibit only a single

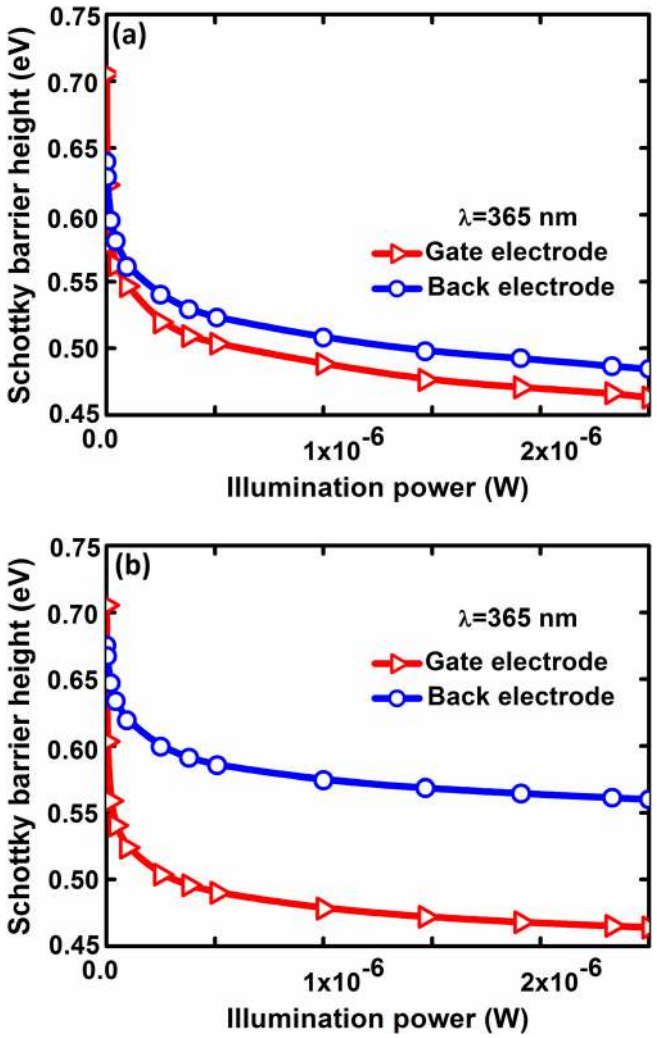

FIG. 8. The influence of illumination intensity on the barrier heights of the electrodes (a) symmetric (b) asymmetric illumination. The distances between gate and back electrodes in (a) and (b), respectively, are 5 μm and 135 μm.

negative capacitance peak. Two main reasons cause the negative capacitance: a nonlinear modulation of the conductance of the neutral part of the semiconductor and trapping and detrapping at interfacial states caused by a variation of the minority carrier density. The existence of interfacial traps enhanced by the filamentation process and additional defects due to the embedded Pt NPs as well as the use of Schottky type contacts are imperative for the appearance of negative capacitance in the MISM structures we have discussed. The supplementary role of Pt NPs is exhibited in the enhancement of the photo generated minority carriers in the depletion regime. This causes an enhancement of the conductance modulation and therefore of the negative capacitance peak values. The effect of Pt NPs on the increase of the light absorption in the semiconductor has been demonstrated before via improvement of the responsivity of photodetectors based on similar structures.[6,21]

A sensitivity of the negative capacitance and conductivity to illumination in a single device fabricated by standard CMOS technology enables its integration into different types of optoelectronic circuits. The negative capacitance can be utilized for different functions such as compensation of undesired parasitic capacitance, bandwidth enhancement of amplifiers, and equalization filters design without passive inductor.[45] Vibration suppression in synchronized switching where a negative capacitor substitutes for an inductor[46,47] is another application. Finally, a negative capacitor can be used to enhance of the tuning range while simultaneously compensating for a series resistance in monolithic microwave integrated circuit varactors.[48]

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