Optically sensitive devices based on Pt nano particles fabricated by atomic layer deposition and embedded in a dielectric stack

V. Mikhelashvili, R. Padmanabhan, B. Meyler, S. Yofis, G. Atiya, Z. Cohen-Hyams, S. Weindling, G. Ankonina, J. Salzman, W. D. Kaplan, and G. Eisenstein

Citation: Journal of Applied Physics **118**, 134504 (2015); doi: 10.1063/1.4932031
View online: http://dx.doi.org/10.1063/1.4932031
View Table of Contents: http://aip.scitation.org/toc/jap/118/13
Published by the American Institute of Physics

Optically sensitive devices based on Pt nano particles fabricated by atomic layer deposition and embedded in a dielectric stack

V. Mikhelashvili,[1,2] R. Padmanabhan,[1,2] B. Meyler,[1] S. Yofis,[1] G. Atiya,[3,2]
Z. Cohen-Hyams,[3,2] S. Weindling,[1] G. Ankonina,[2,4] J. Salzman,[1] W. D. Kaplan,[3,2]
and G. Eisenstein[1,2]
[1]*Electrical Engineering Department, Technion, Haifa 3200, Israel*
[2]*Russell Berrie Nanotechnology Institute, Technion, Haifa 3200, Israel*
[3]*Department of Material Science and Engineering, Technion, Haifa 3200, Israel*
[4]*Photovoltaic Laboratory, Technion, Haifa 3200, Israel*

(Received 29 May 2015; accepted 17 September 2015; published online 6 October 2015)

We report a series of metal insulator semiconductor devices with embedded Pt nano particles (NPs) fabricated using a low temperature atomic layer deposition process. Optically sensitive nonvolatile memory cells as well as optical sensors: (i) varactors, whose capacitance-voltage characteristics, nonlinearity, and peak capacitance are strongly dependent on illumination intensity; (ii) highly linear photo detectors whose responsivity is enhanced due to the Pt NPs. Both single devices and back to back pairs of diodes were used. The different configurations enable a variety of functionalities with many potential applications in biomedical sensing, environmental surveying, simple imagers for consumer electronics and military uses. The simplicity and planar configuration of the proposed devices makes them suitable for standard CMOS fabrication technology. © *2015 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4932031]

I. INTRODUCTION

Metal-Insulator-Semiconductor (MIS) capacitor structures comprising a double layer insulator stack, a thin thermal SiO_2, and a thick atomic layer deposited (ALD) HfO_2, fabricated on either bulk silicon or Silicon-on-Insulator (SOI) substrates, serve as a basis for a variety of electronic and optoelectronic devices. A voltage stress process, which causes filamentation in the dielectric and hence introduces a current leakage path, transforms those capacitors into photodetectors and optically controlled varactors which are highly sensitive over a broad spectral range.[1,2] The photo-detectors, so obtained, exhibit low dark currents and high responsivities in the wavelength range from 245 nm to 880 nm,[1,2] and the optically controlled varactors offer very large capacitance tuning ratios for moderate illumination intensities.[2]

The addition of semiconductor or metal nano particles (NPs) placed between the two dielectric layers changes the capacitors into nonvolatile memory (NVM) cells with very large memory windows, where the NPs serve as effective charge storage nodes[3–8] with the hysteresis being controllable by illumination.[8,9]

This paper described detailed studies of MIS devices that contain Pt NPs fabricated using a low temperature ALD process. Pt was chosen as the NP material due to its large work function difference with silicon that ensures well confined electrons and holes.[3,4,10] The large ratio between the potential well depth and the Coulomb charging energy increases the density of trapped charges per particle.[4,8]

The most common process to form metal NPs starts with the evaporation of a thin metal film which undergoes high temperature (600 °C–800 °C for Pt) rapid thermal annealing (RTA).[4–6] Annealing initiates dewetting[4] which results in an ensemble of small particles having average diameters of 4–5 nm which are fully separated from each other. Using this process in conjunction with SOI substrates introduces a problem stemming from the poor thermal properties due to the thick SiO_2 box layer separating the device layer from the bulk silicon. Under the high temperature process, contaminants migrate to the interfaces between NPs and both insulator layers, which causes an enhancement of the charge/discharge processes due to local states outside the NPs.[8] Additionally, the Pt NPs may react with the SiO_2 sublayer resulting in Pt silicide[11] which thins, in turn, the effective tunneling layer. Above and beyond that, the Pt NPs can actually migrate into the SiO_2 layer further shrinking the tunneling layer.[8] This is clearly seen in Fig. 1(a), which shows a high resolution cross section transmission electron microscope (HRTEM) image of RTA processed Pt NPs, embedded between SiO_2 and HfO_2 layers processed on a SOI substrate.

An alternative process to form Pt NPs is to fabricate them *in-situ* with the HfO_2 layer by ALD. The low temperature (300 °C) ALD process ensures that the NPs do not migrate into the SiO_2 layer and the *in-situ* process avoids contamination stemming from moving the sample between processing systems. A cross section HRTEM micrograph, Fig. 1(b), clearly shows the Pt NPs placed on top of a 2.9 nm thick SiO_2 tunneling layer.

A plan-view image of the NPs obtained from a high resolution scanning electron microscope (HRSEM) is shown in Fig. 2(a). Fig. 2(b) describes a histogram of the NP size distribution measured for approximately 900 particles. More than 60% of NPs' diameter of these ALD processed Pt NPs is 4–5 nm, approximately the same as the sizes of typical NPs fabricated by RTA.

The low temperature technique to form Pt nanoparticles was reported in Refs. 12 and 13 and was used effectively for improved catalysts and catalytic fuel cells.[14,15] A

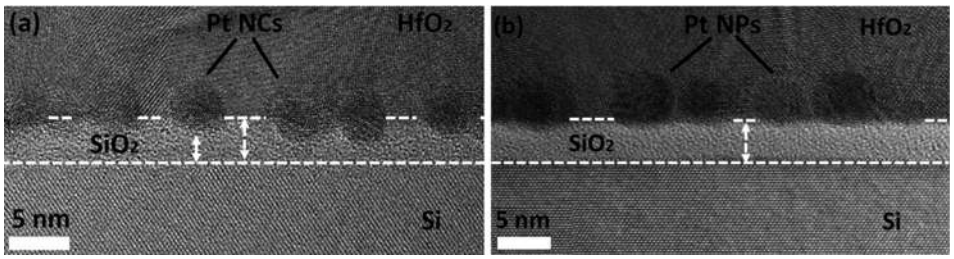

FIG. 1. Cross-section HRTEM micrographs of Pt NPs in a NVM capacitor fabricated on a SOI substrate. The HRTEM images were obtained using a monochromated and aberration-corrected FEI Titan 80–300 kV S/TEM microscope with a measured spatial resolution of 0.07 nm (in TEM mode). (a) RTA processed NPs. (b) ALD processed NPs. The arrows denote the effective thickness of the oxide layer. The small arrow in Fig. 1(a) denotes the effective thinning of the tunneling SiO_2 due to the embedded Pt NPs.

non-volatile memory MIS structure fabricated on a bulk silicon substrate that used ALD Pt NPs embedded between a 6 nm thick thermal SiO_2 tunneling layer and an HfO_2 blocking layer which was annealed at 450 °C for 5 min was reported in Ref. 16. The thick tunneling layer ensured good retention properties, and the entire process lends itself to standard CMOS processing. However, no previous work addressed the use of a SOI substrate in conjunction with ALD processed NPs. SOI substrates have significant advantages due to their widened spectral response[1,2,17,18] and the low temperature process adds a major improvement as clearly seen in Fig. 1.

We describe first a systematic study of NVM MIS capacitors with embedded Pt NPs fabricated by ALD. The capacitors were characterized in the dark and under illumination. These capacitors were also voltage stressed, turning them into optically sensitive varactors and photo detectors. The nonlinear behavior of the current-voltage and capacitance-voltage characteristics of these voltage stressed devices was studied. The dependence on illumination intensity and measurement frequency of single devices as well as back to back connected pairs of diodes (which exhibit bipolar hysteresis characteristics) was measured. The key role played by the Pt NPs was clearly identified.

II. EXPERIMENTAL PROCEDURE

Planar MIS structures were fabricated on a SOI substrate comprising a 2.9 μm thick phosphorous doped n-Si layer with a resistivity of 90 Ω cm, grown on top of a 1.3 μm thick SiO_2 spacer. The thickness of the silicon device layer was chosen based on Ref. 17. Spectroscopic ellipsometry was employed to measure the wavelength dependent extinction coefficient $(k(\lambda))$ of a Si device layer covered with a 2.9 nm thermal SiO_2 tunneling film. From $k(\lambda)$, it is straightforward to calculate the absorption coefficient and light penetration depth which are shown in Fig. 3(a) as red and blue traces, respectively.

Such a SOI substrate avails a measurable photo sensitivity in the range of 245 nm to at least 880 nm. The 2.9 nm thickness of the thermal SiO_2 tunneling layer was shown in Refs. 1 and 2 to be optimal when followed by a 20 nm ALD HfO_2 blocking layer. It enables a controllable filamentation process of the dielectric stack at moderate stress voltages and yields low dark currents in the photodetectors. Nevertheless, the 2.9 nm tunneling layer is thinner than the commonly used value of more than 3.4 nm, which is needed to enact a Fowler-Nordheim tunneling process,[19] and hence, the retention properties of the present device are somewhat inferior.

A ~3 nm thick Pt film was deposited on top of the thermal SiO_2 layer by ALD using (Trimethyl)methylcyclopentadienylPlatinum (IV) ($MeCpPtMe_3$) in an oxygen environment and at a substrate temperature of about 300 °C. The thin Pt film cannot maintain a homogeneous form and breaks up into an ensemble of individual particles which are separated from each other as shown in Fig. 2(a). These Pt NPs were subsequently covered by a 20 nm thick HfO_2 blocking layer deposited *in-situ* by the ALD system.

Spectroscopic ellipsometry measurements were also used to extract the absorption coefficient and penetration depth spectra of the entire structure (Si device layer, SiO_2 tunneling layer, and the HfO_2 blocking layer) with and without the Pt NPs. The enhancement of the absorption coefficient due to the Pt NPs is moderate but is clearly seen in the wavelength range of 400–500 nm. The enhancement is

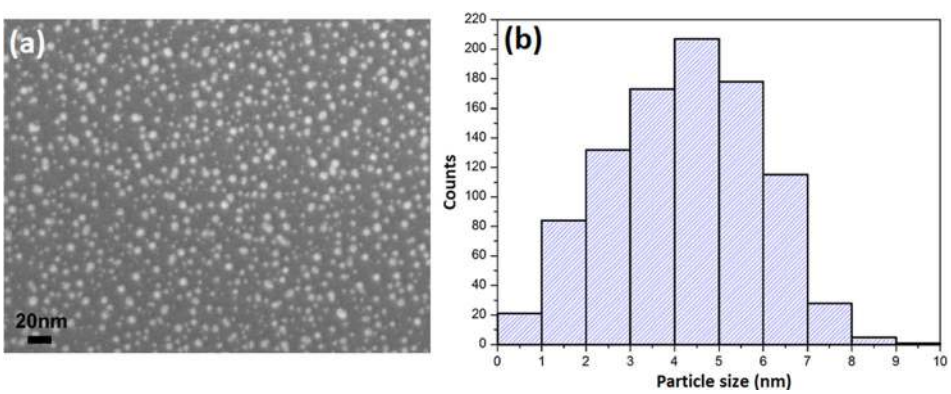

FIG. 2. (a) Plan-view HRSEM of Pt NPs fabricated by ALD. The HRSEM images were obtained by a Zeiss Ultra-Plus FEG-SEM. (b) Histogram of the size distributions.

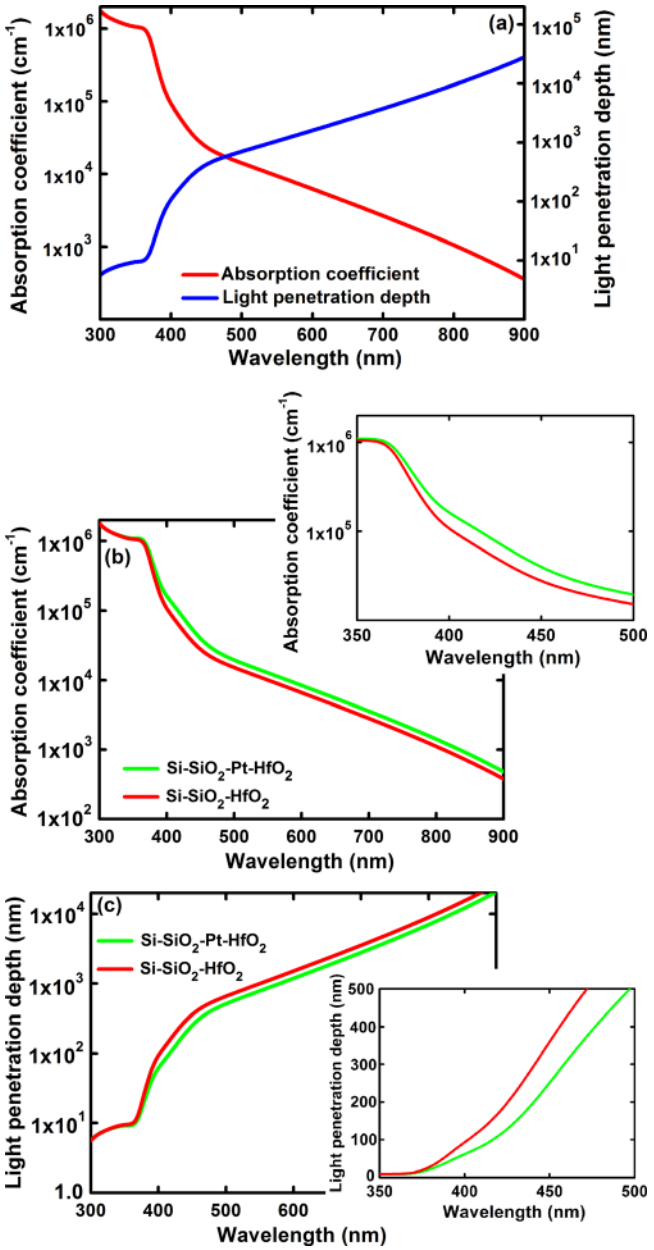

FIG. 3. Absorption coefficient and penetration depth spectra obtained from spectroscopic ellipsometer measurements using model V-VASE ellipsometer (J. A. Woollam Co. Inc.) in the 300–1000 nm wavelength range at 65°, 70°, and 75° angles of incidence. (a) Si device layer. (b) and (c) Comparison of a Si-SiO_2-Pt NP-HfO_2 and a Si-SiO_2-HfO_2 structure; (b) absorption coefficient and (c) penetration depth spectra. The inserts in are zoom images in the 350 nm to 500 nm wavelength range.

highlighted in the two insets which are zoom images of the 350–500 nm wavelength range. The reason behind the improvement was not fully clarified. A plasmonic enhancement was ruled out due to the small size of the NPs. A possible reason is a slight change in the effective refractive index of the dielectric stack and a consequent enhanced transmission through it which practically enhances the absorption.

Similar base structures but with a tunneling oxide thickness of 3.2 nm and 3.6 nm were fabricated simultaneously on a boron doped bulk p-silicon substrate. Diodes were constructed by depositing Ti/Pd/Pt/Au stacks for both gate and back contact electrodes in the SOI based structures, while, for the devices based on bulk substrates, Ti/Pd/Pt/Au electrodes comprised the gate contacts and Al was used for the back contact electrodes. The filamentation paths in the dielectric stack were obtained by voltage stressing the capacitors using several ms long pulses with an amplitude of slightly below 12 V, which is close to, but lower than, the voltage causing hard breakdown.

A schematic cross section of the device is shown in Fig. 4. The optical input port is the area between the center gate contact (whose area is 7.85×10^{-5} cm^2) and the ring back contact. The area of the optical window was 1.225×10^{-4} cm^2.

III. RESULTS

The experimental set-up is described schematically in Fig. 4(b). Current-voltage (I-V) characteristics were measured using an Agilent 4155C Semiconductor parameter analyzer. Capacitance-voltage (C-V) characteristics were obtained from an HP4192A LF impedance analyzer; for single devices, it was operated in the parallel mode, while for two back to back connected diodes, we employed the series impedance mode. The optical characterization used a light emitting diode (LED) array which avails collimated illumination in the 265–880 nm wavelength range. The LED output was coupled to the diode under test via a lensed fiber or a large curvature lens. The corresponding illumination spot areas for the fiber and lens were 8.1×10^{-6} cm^2 and 4.9×10^{-2} cm^2, respectively.

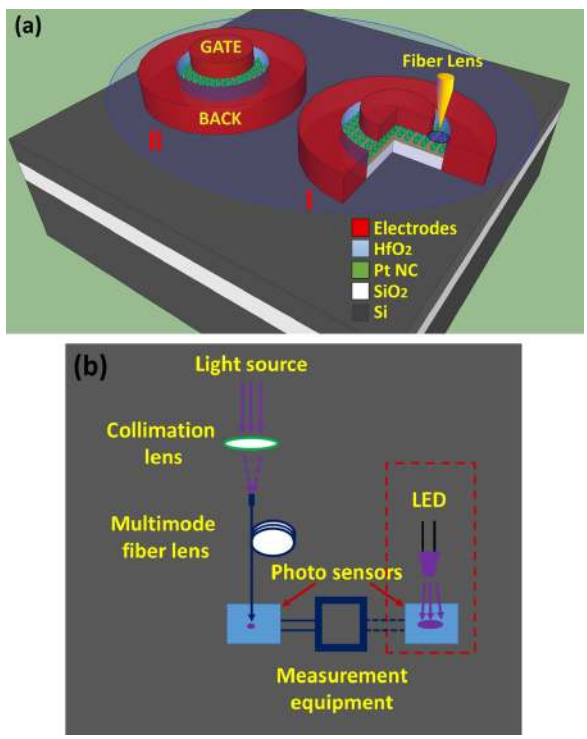

FIG. 4. (a) Schematic cross section of the device structure. (b) Schematic diagram of the experimental setup. Contours of the illumination spot are marked by a large and a small ellipses, for the large curvature lens and the fiber, respectively.

A. NVM MIS diodes containing ALD Pt NPs

Measured C-V characteristics of an unstressed capacitor are presented in Fig. 5(a). Shown are clockwise curves measured in the dark and under illumination via a fiber lens. The characteristics are similar to ones reported in Ref. 8. Fig. 5(b) shows for comparison C-V characteristics of a diode which contains no NPs. Sweeping the bias over 5 V yields a small hysteresis window of only 0.4 V and 0.6 V in the dark and under illumination, respectively. This slight hysteresis is due to the presence of uncontrolled bulk or interface state traps, which are often found in HfO_2-based MIS structures.[20] The large difference between the C-V curves highlights the role of the Pt NPs as charge trapping nodes in non-volatile memory process independently on the illumination regime.

Returning to the diode with the Pt NPs, starting from positive bias, an accumulation layer is formed in the n-type Si. The electric field is directed from the gate electrode towards the accumulation layer, and electrons are injected through the tunneling oxide towards NPs where they are trapped and charge them negatively. Hole injection from the NPs is insignificant due to their large barrier height. As the bias is lowered toward zero, electron flow through the tunneling layer and their trapping in the NPs are reduced. A bias level smaller than the flat band voltage causes a reduction of the total capacitance due to a change in the band bending direction at the boundary; the electric field decreases across the tunneling oxide thereby lowering the electron tunneling probability through the oxide layer.

As the bias becomes negative, the depletion layer width increases forming an inversion Si layer rich with holes. The electric field is directed now from the inverted layer towards the gate electrode; the holes from the inversion layer penetrate through the tunneling layer and are trapped by the NPs, while released electrons move in the opposite direction. The C-V characteristics shift in the negative bias direction due to the positively charged NPs. As the absolute value of the applied voltage decreases below of the new flat band voltage value, the accumulation capacitance increases and effects due to the inversion are reduced. The resulting hysteresis loop has a width which is determined by the NP density, the probability of the tunneling process, and the sweeping voltage.

Trapped holes or electrons can be stored in the Pt NPs for a long time due to the three dimensional carrier confinement which is responsible for the large work function difference between Si (4.05 eV) and the Pt nanocrystals (5.3–6.35 eV).[21,22] The leftward shift of the C-V characteristics, under dark conditions, is limited (compared to the right side) by the low minority carrier (holes) density in the

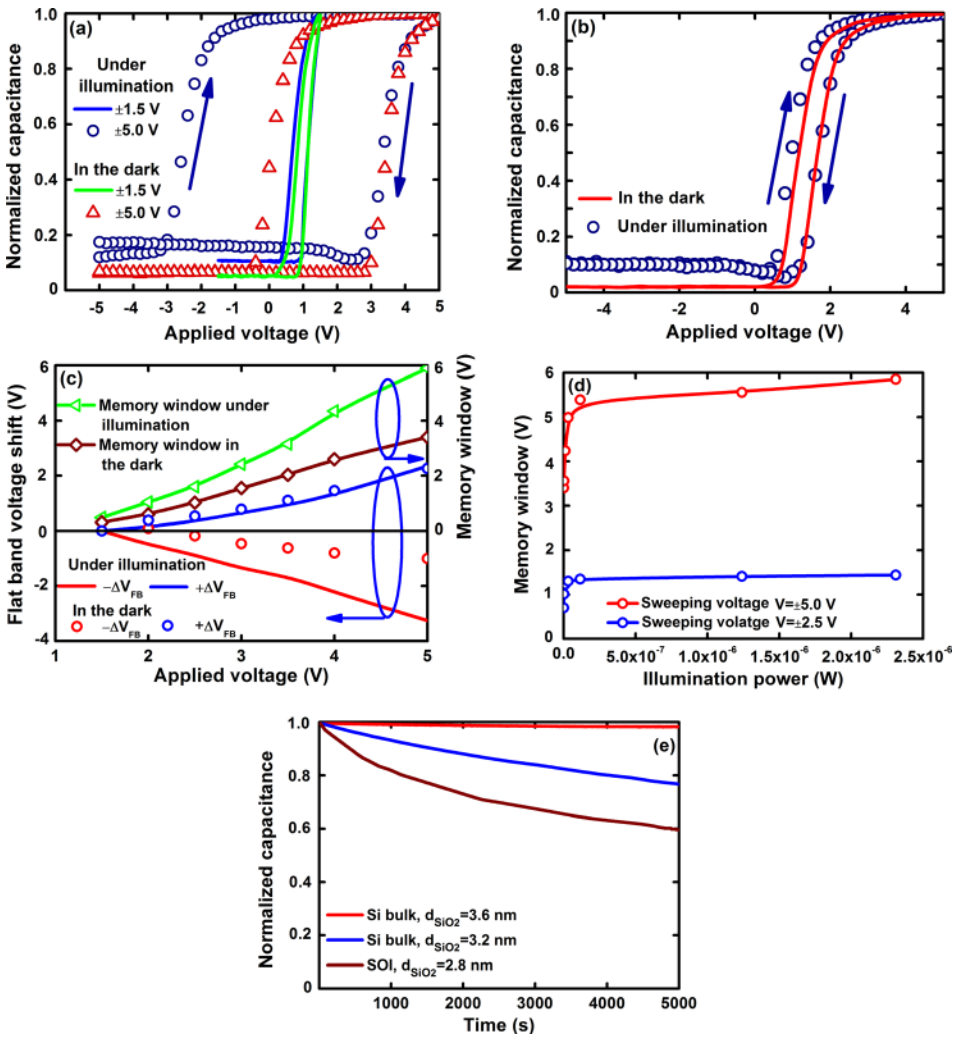

FIG. 5. Unstressed single NVM structure. (a) Normalized C-V characteristics measured for different sweeping voltage in the dark regime and under illumination via a fiber lens at an intensity of 2.3 μW at 365 nm. The arrows denote the clockwise voltage sweep direction of the hysteresis loops. (b) Normalized C-V characteristics of structure without Pt NPs measured in the dark regime and under illumination via a fiber lens at an intensity of 2.3 μW at 365 nm. (c) Flat band voltages shift and hysteresis width measured at positive and negative gate voltages in the dark and under illumination. (d) Illumination dependent memory window measured at different sweeping voltages. (e) Normalized capacitance decay for NVM structures based on SOI and bulk Si substrates with different thicknesses of the tunneling SiO_2 layer.

inversion layer. This condition can be changed by an increased temperature or by illumination. Illumination enlarges the leftward shift of the C-V characteristics and therefore increases the net width of the memory window, as seen in Fig. 5(a).

The electric field causes a separation of photo generated electron-hole pairs. Those generated in the intrinsic region tunnel directly to the NPs while carriers generated in the semiconductor bulk diffuse through the depletion layer to the inversion layer. The density of photo-generated holes injected from the inversion layer increases the population of charged Pt NPs and this widens the hysteresis loop in the negative bias direction. The resulting flat band voltage depends on the light intensity and the wavelength. This manifests itself in a symmetric expansion of the hysteresis for both bias polarities, in contrast to the case of the dark regime. Fig. 5(c) summarizes the dependencies on illumination of the flat band voltage shift and therefore on memory window. At the maximum applied voltage, the measured memory window is about 1.7 times larger under illumination than in the dark regime.

The total charge density in the Pt NPs for both bias polarities can be calculated using the standard equation: $N_{charge} = \Delta V C_{contr}/qS$ where q is the electron charge, C_{contr} is the capacitance of the HfO_2 blocking layer (with a dielectric constant of 21) and S is the gate electrode area. At a gate voltages of ± 5 V and a capacitance density $C_{contr}/S = 9.3 \times 10^{-7}$ Fcm^{-2}, N_{charge} is approximately 2×10^{13} cm^{-2} in the dark and 3.3×10^{13} cm^{-2} under an illumination power of 2.3 μW.

The number of the electrons trapped by a single Pt NP under positive bias can be calculated in accordance with Ref. 4 using $\upsilon = d_{eff}/\Delta E_g$, where $\Delta E_g = q^2/C_{self}$ is the Coulomb energy gap. $C_{self} = 2\pi\varepsilon_{tun} d_{nc}$ is the self-capacitance, ε_{tun} is the dielectric constant of the tunneling insulator ($\varepsilon_{tun} = 3.9$), and d_{nc} is mean size of the NPs. d_{eff} is the effective potential well depth equal to the work functions difference between the Si substrate and the NPs. This difference takes on the values 1.25 eV to 2.3 eV, depending on the work function of Pt which can vary from 5.3 eV to 6.35 eV for bulk Pt.[21,22] Ref. 22 showed that for 1.8 nm Pt NPs, the effective work function is 5.95 eV, quite close to that of bulk Pt. Considering the average size of the Pt NPs to be $d_{nc} = 4.5$ nm, ΔE_g is roughly 0.16 eV. Therefore, the number of electrons trapped per Pt NP can vary from 8 to 15. Employing the plan-sphere capacitance model[22,23] yields $\Delta E_g = 0.131$ eV, and therefore, the number of trapped carriers per Pt NP is between 10 and 18. Both models assume a uniform size distribution of the NPs which is not satisfied in practice (see Fig. 2), and therefore, it is not possible to identify quantitative differences between the models and both yield only general trends.

The influence of illumination on the evolution of the total memory window, measured at two bias levels, ± 2.5 V and ± 5 V, is described in Fig. 5(d). A significant increase of the memory window occurs at small illumination levels and this increase saturates fast, consistent with Refs. 9 and 24. The bias level determines the nominal memory window but the general dependence on illumination is bias independent.

The retention properties of the NVM capacitor are described in Fig. 5(e) (brown trace). The temporal evolution of the capacitance, measured in the dark under zero bias and after being charged at $+5$ V for 2 s, exhibits an initial decrease by 20% during the first 1000 s and starts to saturate reaching 60% of its initial value after 5000 s.

The initial fast capacitance decay is a result of lateral charge migration between neighboring NP sites,[25] which is enhanced by the fact that the distance between NPs is non uniform and since the distribution of interfacial defects is random. A second possible reason of the initial loss of carriers are traps which are induced by defects due to compressive strain near the interfaces of the NPs and the dielectric films between which they are embedded. The possible formation of a transition interface layer was discussed in Ref. 26. The slow decay is caused by back tunneling of trapped charges to the substrate through the thin SiO_2 layer.[19] Another possible reason for the loss of retention was suggested in Ref. 27, where a similar insulator stack, but with embedded Au NPs, was studied. It was established that poor retention characteristics result from loss of carriers trapped in the NPs that tunnel through the blocking HfO_2 layer to the gate electrode assisted by traps related to the oxygen vacancies. These oxygen vacancies result from the breaking of Hf-O chemical bonds.[27] Moreover, when the blocking layer is grown on top of the NPs, the initial atomic layers of the HfO_2 covering the NPs grow as a porous rather than a continuous film[28,29] with a large stoichiometric deficiency of oxygen. This can lead to an additional loss of trapped carriers.

The parallel shift in the C-V characteristics (without a "stretch-out" effect) towards the negative voltage side of structure without Pt NPs (see Fig. 5(b)) in both measurement regimes indicates the generation of a relatively small amount of interface traps related of border-states,[30] while the hysteresis is related to the bulk traps induced by the oxygen vacancies.

The retention properties can be improved by increasing the tunneling layer thickness. This is demonstrated in Fig. 5(e) by the blue and red traces which describe capacitance decay characteristics of NVM capacitors having the same ALD processed NPs but fabricated on a bulk Si substrate with 3.2 nm and 3.6 nm SiO_2 layers, respectively. For the 3.2 nm thick oxide layer, the capacitance reduces by 20% from its initial value after 5000 s, while with a 3.6 nm thick tunneling oxide, it drops by only 2%–3%. These retention properties are comparable to those obtained with RTA processed NPs reported in Refs. 6 and 16.

The erase and write voltages were -5 V and $+5$ V for all the experiments described in Fig. 5 with the erase process lasting 50 s. The few Angstroms difference in the tunneling oxide thickness is responsible for the retention enhancement; in that sense, ALD and RTA NPs are very similar. The write time in the bulk devices is longer than for the SOI case, also because of the thicker tunneling layer which dictates that charging of the NPs is via Fowler-Nordheim tunneling while in the SOI case, charging is by the more efficient direct tunneling process through the thinner SiO_2 layer.

B. Optically sensitive voltage stressed MIS diodes containing ALD Pt NPs

The SOI based diodes with the ALD processed NPs were voltage stressed using a bias of 12 V similar to Refs. 1 and 2. The stressed diodes were tested as optically controlled varactors in a single device configuration and as a back to back pair of devices.

The C-V characteristics of a single voltage stressed device, measured in the dark and under illumination for voltage sweeps in either direction, are shown in Figs. 6(a) and 6(b). The two C-V curves are mirror images of each other, each containing an illumination dependent peak, at positive bias, and a bend which evolves with illumination. The curves exhibit an obvious hysteresis which is smaller than that in the unstressed NVM capacitor.

Fig. 6(c) shows the voltage sensitivity, $Slope = d\ln C/d\ln V$, which is the rate of change in the capacitance versus voltage function within the tuning range. The slope is shown to be vastly enhanced with illumination and to depend on the voltage sweep direction.

The peak capacitance dependence on illumination intensity is shown in Fig. 6(d) for both sweeping voltage directions. The peak capacitance changes by a factor of 3 between the dark and an illumination intensity of 2.3 μW for the negative to positive sweeping direction (where the peak occurs at +0.6 V), while for the opposite sweep direction, the peak is at +0.2 V and increases by a factor of 11. The different ratios stem from differences in the minimum value of the depletion capacitance for the negative and positive applied voltages, respectively, seen in Figs. 6(a) and 6(b), respectively.

The maximum change in capacitance with voltage,[31] C_{max}/C_{min}, under a constant illumination power of 2.3 μW was 25 relative to any negative bias below −1.5 V, and 5 relative to a positive bias above +1.5 V. These ratios are independent of the voltage sweep direction.

C-V characteristics of similar structures but without the embedded Pt NPs, which exhibit a hump (near zero bias) and a peak (at positive voltages) were discussed in Ref. 2. Changes in the capacitance with frequency and illumination intensity were attributed to thermal or photo generated

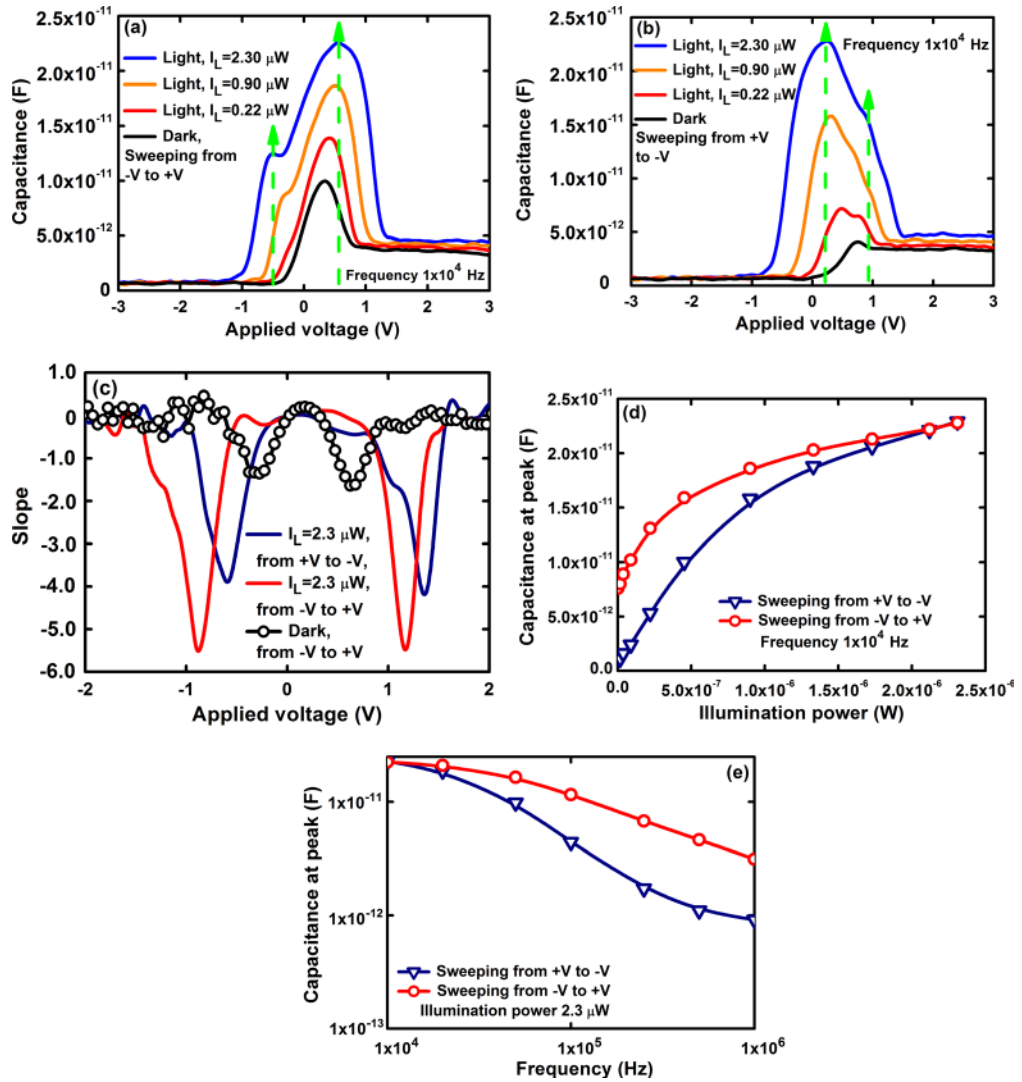

FIG. 6. Voltage stressed single diode. (a) and (b) C-V characteristics of a varactor measured for two voltage sweep directions in the dark and under illumination. (c) Slopes of C-V characteristics for two voltage sweep directions in the dark and under illumination. (d) Illumination power dependent peak capacitance for the two sweeping voltage directions. (e) Peak capacitance dependence on the measurement frequency of the C-V characterization system measured under illumination for two sweeping voltage directions. The illumination in all experiments was at 365 nm.

carrier charging and discharging processes, consistent with Refs. 32–35. Similar dependencies originate also from intrinsic or artificial (induced by the voltage stressed process) traps located at the dielectric-semiconductor interface or placed inside the dielectric stack and distributed throughout wide dielectric band gap. In the present devices, there are additional effects since traps formed by Pt NPs embedded in the dielectric stack play a major role in modifying the peak capacitance due to changes in their charge state as they capture or emit electrons or holes whose generation rate varies with frequency and illumination intensity. Additionally, changes in the trapping and de-trapping process of the Pt NPs due to photo generated carriers shift the peak location with sweeping voltage directions and therefore causes a hysteresis in the C-V curves.

The origin of the capacitance bends, located at bias levels far from zero, are similar to those observed in forward biased MS-MS or MS-MIS structures,[2,36–41] but its behavior under illumination differs in the present devices. Additionally, the location of the bend changes here with the sweeping voltage direction, while in structures without NPs, it was observed only at positive bias.[2]

The peak capacitance dependence on the measurement frequency used in the C-V characterization system, under an illumination intensity of 2.3 μW, is shown in Fig. 6(e) for both sweeping directions. Observation of the complete C-V curves reveals that even at 100 kHz the general shape of the C-V curves remains unchanged. In the range of 10 kHz to 1 MHz, the capacitance changes by a factor of 25 for the positive to negative sweep direction and by a factor of only 7.2 for the opposite direction. The dissimilar frequency responses are due to the different depletion region widths of the device Si layer located under the back and gate electrodes which determines the minority carrier density. Differences in minority carrier densities generated in the depletion regions, their ability to follow high frequency signals, and hence to contribute to the NPs charging processes all limit the high frequency capacitance values.

A more interesting varactor configuration is based on two diodes connected back-to-back via the silicon device layer with their gate electrodes being driven by the double sweep directed voltages. This configuration was tested with one diode (number I) under illumination while the second (number II) is in the dark or with both illuminated simultaneously (see Fig. 4). In all cases, the applied voltage polarity and therefore sweep directions of the C-V curves relates to diode number II. The characteristics of the back to back configuration are described in Fig. 7.

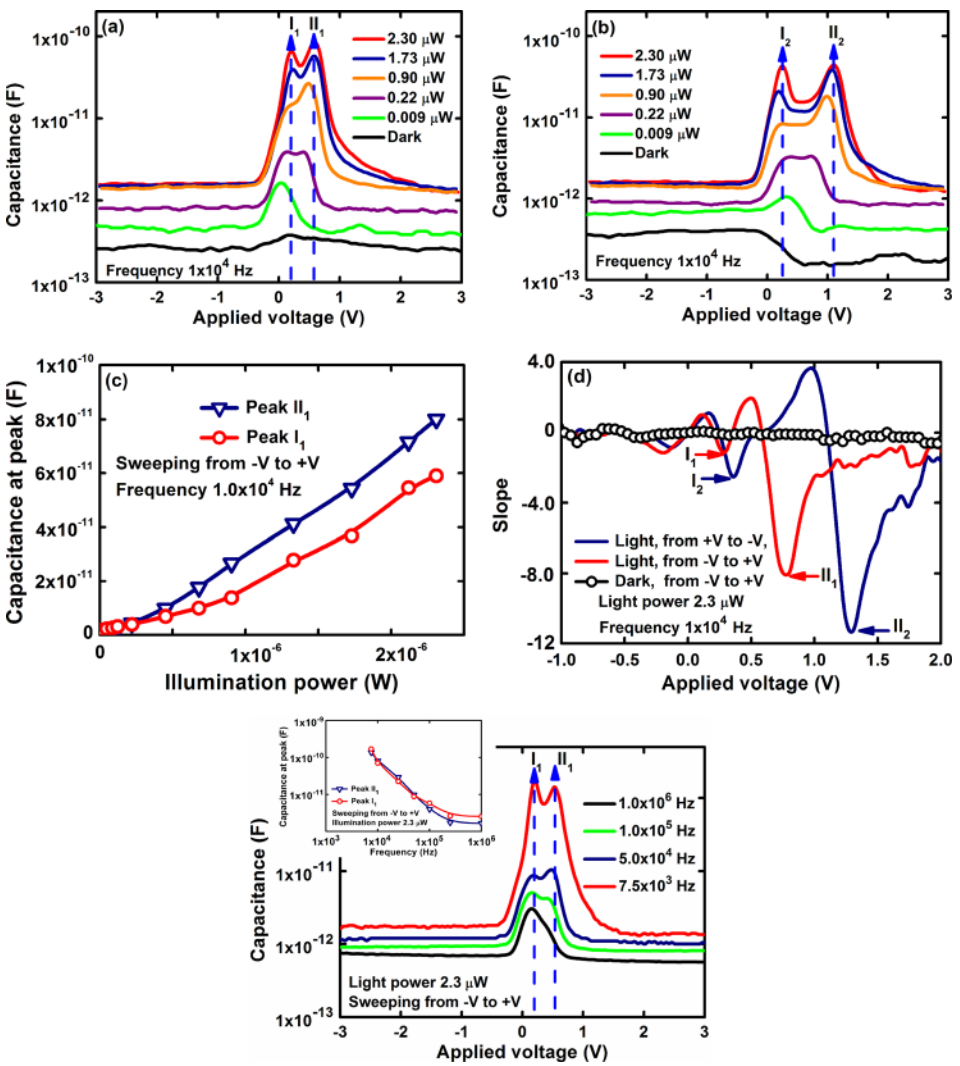

FIG. 7. Back-to-back connected voltage stressed diodes with only diode I being illuminated at 365 nm. The voltage on diode I is constant and in diode II (which is in the dark) it is variable. (a) and (b) C-V characteristics of a system measured for two voltage sweep directions in the dark and under illumination. (c) Illumination power dependent peak capacitances for negative to positive sweep voltage direction. (d) Slopes of C-V characteristics for two voltage sweep directions in dark and under illumination. (e) C-V characteristics measured at different frequencies and under constant illumination power for sweep voltage direction from negative to positive. The inset shows the frequency dependences of the peak capacitances.

The C-V characteristics measured at 10 kHz and under various illumination intensities of one diode (diode I) is shown in Fig. 7(a) for a negative to positive voltage sweep direction and Fig. 7(b) for the opposite direction. For large illumination powers, the characteristics differ significantly from those of the single diode of a similar configuration having no Pt NPs reported in Ref. 2. The main difference is the appearance of two peaks which are separated by a valley. The separation of these peaks and the peak to valley ratio depend on the voltage sweep direction. The maximum peak to valley ratio at an intensity of 2.3 μW was 2.52 when sweeping from positive to negative voltage and 1.71 in the opposite direction. On both sides of the peak, the capacitance drops to similar levels, which are limited by the capacitance of the depletion regions under the corresponding electrodes.

The peak capacitance dependence on illumination for the negative to positive sweep direction is shown in Fig. 7(c). The dependence is super linear in the 0.5 to 2.3 μW intensity with the ratio C_{light}/C_{dark}, reaching a level of 175 and 250–280 for the two peaks under an illumination of 2.3 μW; this is almost two orders of magnitude larger than in the single device case. When sweeping from positive to negative voltage, the peak dependence on intensity is also super linear and the C_{light}/C_{dark} ratio exhibits similar levels.

Fig. 7(d) describes the voltage sensitivity of the C-V slope in the dark and under illumination at 2.3 μW for both directions of the voltage sweep. The maximum slopes are 8 (for a negative to positive voltage sweep) and 12 for the opposite direction; these values are two times larger than those for a single device. Finally, we extract from Figs. 7(a) and 7(b) the maximum capacitance change at a given illumination intensity. For 2.3 μW, $C_{\max}/C_{\min}$ takes on the values of 47.5 and 25 for the right peaks I_2 and II_2 in Figs. 7(a) and 7(b) and 41 and 26 for the corresponding left peaks I_1 and II_1. These values are more than two times larger than for a single device under the same illumination intensity.

C-V characteristics obtained for different measurement frequencies, in the negative to positive bias direction, are shown in Fig. 7(e). The double peak nature of the characteristics holds here for measurement frequencies as high as 100 kHz. The inset in Fig. 7(e) shows the frequency dependence of each peak of the response.

The C-V characteristics of a pair of back-to-back connected diodes which are illuminated simultaneously through a large curvature lens are shown in Fig. 8(a). The C-V curves are symmetric and double peaked for both bias polarity, similar to Figs. 7(a) and 7(b), which relate to only one diode being illuminated. A clear hysteresis is observed also here when sweeping in the two bias directions.

A somewhat similar behavior of the C-V characteristics but with a single peak followed by a valley was observed in a structure with planar double gate electrodes on LaAlO(3)/SrTiO(3),[42] where a peak to valley ratio of 1.4 was observed at a frequency at 5 kHz in the dark regime. Devices with two parallel quantum wells having tunable concentrations of a two-dimensional electron gas, obtained by applying a bias on separate electrodes, were considered theoretically in Ref. 43 and predicted a similar behavior. This concept was realized in a metal-semiconductor-metal structure with

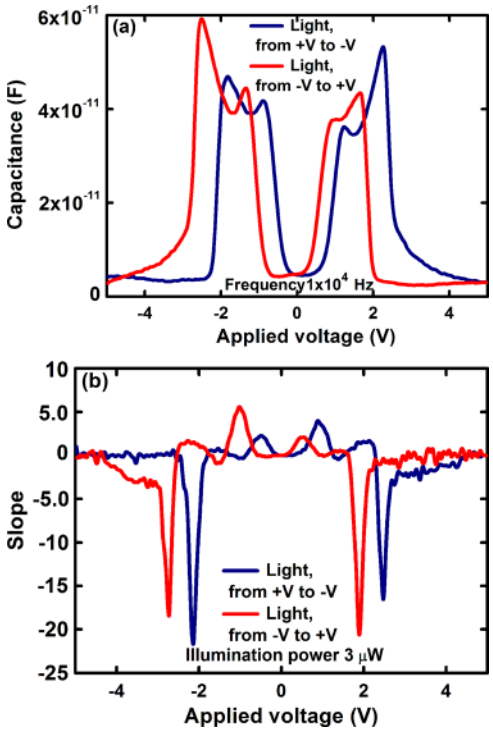

FIG. 8. C-V characteristics measured for two voltage sweep directions under constant illumination power for a back-to-back connected voltage stressed diodes with both diode illuminated using a large curvature lensed LED with an intensity of 9 μW at a wavelength of 365 nm. The voltage on diode I is constant and in diode II it is variable.

embedded separate electrodes. A two dimensional hole system was illuminated and yielded a light sensitive capacitor.[44] This varactor operated well at low frequencies and with a low product of electron density and inter electrode distance. Changes in voltage or illumination intensity manipulate the quantum state of the two dimensional charge system resulting in a sharp peak in the C-V curves. The peak occurs at critical charge densities corresponding to a transition from metallic (carriers accumulation) to insulating (carriers depletion) states of the two dimensional system. We postulate that the Pt NP layer in the present devices can also play an analogous role to the two dimensional system as it is charged and discharged by photo generated carriers.

An additional factor,[36–39] discussed in Ref. 2 that may explain the sharp capacitance reduction near the main peaks (in either voltage polarity, see Figs. 7 and 8) is due to the series resistance of the device.[38] Under forward bias, the minority carriers from the electrode are injected into the bulk Si, where they either recombine or drift toward the reverse biased back electrode where they are extracted. A reverse bias initiates a minority carrier drop (sink) in the valence band edge of the Si, an effect which enhances the ability of the back contact to extract the minority carriers. This reduces the resistance, which yields, in turn, the increase of value of the capacitance peak at forward bias. Illumination enhances the generation of the minority carrier concentration and significantly modifies the resistance and therefore cause the change in peak capacitance.

The maximum capacitance change C_{light}/C_{dark} seen in Fig. 8 is more than 400 at an illumination power of 9 μW,

where the dark capacitance is about $1.3-1.5 \times 10^{-13}$ F, independent of sweeping voltage directions, too low to be shown in Fig. 8. The peak to valley ratio is about 10, independent of the sweeping voltage direction. This ratio exceeds by several times that obtained for a device with a planar metal-semiconductor-metal AlGaAs-GaAs structure that includes a two dimensional hole system.[44] The voltage dependent slope characteristics were extracted from the C-V characteristics and are shown in Fig. 8(b). The slope maxima, 20–23, are two times larger than that in a single diode or in the back to back connected configuration with one diode illumination.

A different back to back configuration which was also examined comprised of one stressed and one unstressed diode. The stressed device was fed with a variable voltage and only it was illuminated. The C-V characteristics, measured at 100 KHz, of such a system are shown in Fig. 9.

The counter-clockwise C-V curves relate to the unstressed, dark, diode. The C-V curves differ significantly from those obtained in voltage stressed single or back to back pair of stressed diodes under illumination. The hysteresis loop resembles characteristics of a single unstressed device from the point of view of the non-volatility. The hysteresis width change with illumination is smaller than in an unstressed diode, but, at the same time, it exhibits an increase of the accumulation and depletion capacitances. This behavior stems from modification of the forward biased stressed diode under illumination. First, photo generated minority carriers, injected from the positive biased stressed diode gate electrode, penetrate the depletion region of the negatively biased unstressed diode. The carrier drift component is much larger here than the diffusion current (due to a large inter gate electrodes distance 500 μm between diodes) which dominates at low bias.[40] These carriers increase the depletion region capacitance of the unstressed diode since they enhance the inversion layer population. Second, illumination modifies the barrier height of the forward biased gate-insulator stack junction more than in Ref. 1 and consequently reduces the differential resistance in series with the unstressed capacitor. Namely, under illumination, alteration of the series resistance is the reason for the change in the accumulation capacitance. The depletion and accumulation capacitances change by factors of 8 and 20, respectively, at an illumination intensity of 2.3 μW, and the consequent accumulation to depletion capacitance ratio changes by a factor of at least two.

C. Photodetection using voltage stressed MIS diodes containing ALD Pt NPs

The single stressed diode and the back to back configuration were tested as photodetectors under different operating conditions. Fig. 10(a) compares the spectral dependence of the photo detector with that of a similar diode that contains no Pt NP. The spectral response is enhanced due to the NPs in the spectral range 265–880 nm, consistent with the increase in the silicon layer absorption measured by ellipsometry and shown in Fig. 3. Fig. 10(b) shows the illumination intensity dependence of the photocurrent for the detector containing the Pt NPs. The response is very linear. The I-V curve (not shown here) reveals a reverse biased dark current of approximately 200 pA.

A back-to-back configuration of the photodetector was also characterized with the common terminal-diode being illuminated while the diode whose bias is varied is kept dark. A measured I-V curve is shown in Fig. 11(a). The dark current is only 70 pA, in both bias polarities, thanks to the large total differential resistance. The symmetry is due to the fact that one diode is always reversed biased, and this diode determines the dark and photo current. The photocurrent dependence on illumination power at 365 nm is shown in Fig. 11(b). The detector is very linear, and the responsivity is 0.215 A/W, which is somewhat lower than in the single diode configuration, but is nevertheless larger than the responsivity for structure with no Pt NPs.

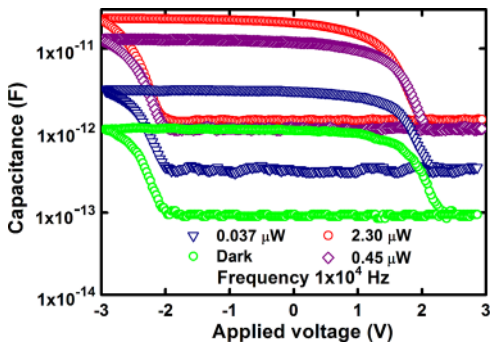

FIG. 9. C-V characteristics of the back-to-back connected voltage stressed and unstressed diodes measured in dark and under illumination at 365 nm. Only the stressed diode is illuminated, and its gate voltage is variable.

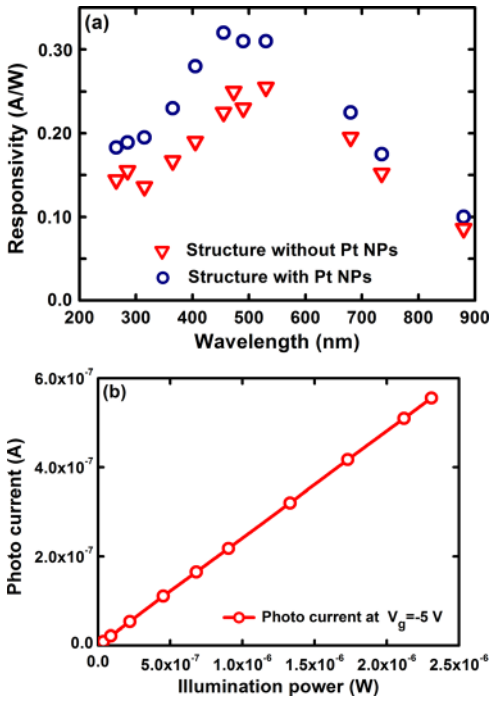

FIG. 10. (a) Spectral responses of photodetectors with and without Pt NPs. (b) Illumination (at 365 nm) dependent photocurrent of a diode containing Pt NPs. The solid line is a linear fit.

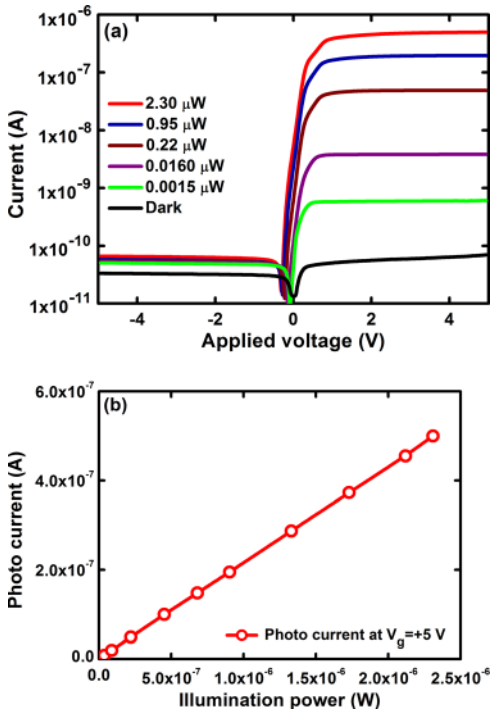

FIG. 11. Photocurrent response of the back-to-back connected stressed diodes with only diode I being illuminated at 365 nm. (a) I-V characteristics in dark and illumination. (b) Photocurrent versus illumination power at a constant positive voltage. The solid line is a linear fit.

IV. CONCLUSIONS

To conclude, we have demonstrated a series of devices all based on an MIS structures with embedded Pt NPs fabricated *in situ* at low temperatures by ALD, with an HfO_2 blocking layer on a thermal SiO_2 tunneling oxide, and all using a SOI substrate. The devices offer various functionalities such as: (i) An optically sensitive non-volatile memory cell realized by a single unstressed MIS structure; (ii) A linear photo detector with a responsivity as high as 0.225 A/W and an external quantum efficiency of 80% (at 365 nm) based a on a single voltage stressed MIS structure; (iii) A back-to-back connected voltage stressed MIS configuration with a very low dark current at both bias polarities; (iv) A capacitance photo sensor based on a single and a back to back pair of voltage stressed MIS structures. C-V characteristics which are independent of the bias sweeping directions were demonstrated. These varactors exhibit a hysteresis due to the charging and discharging processes of the Pt NPs. The maximum light-to-dark capacitance ratio demonstrated was 200, measured at 10 kHz, for the back-to-back connected system. This ratio is more than four times larger than that reported for a planar metal-semiconductor-metal AlGaAs-GaAs structure that includes a two dimensional hole system.[44] This ratio reduces with frequency, but, even at 50 KHz, it is at least 10, five times larger than reported in Ref. 44; (v) A two terminal non-volatile memory system, including back-to-back stressed and unstressed MOS structures that also play the role of a photo sensor which alters the depletion and accumulation capacitance levels when the stressed diode is illuminated. The various devices we reported can be fabricated by standard CMOS technology and can also be the basis for nonvolatile memory field effect photo transistors on SOI.

The various functionalities make these devices attractive for numerous sensing applications ranging from complex military, biomedical, and environmental areas to imagers in consumer electronics where the Si-based broadband photodetectors and optically variable capacitors with the advantages of CMOS-compatible processing and reduced cost are highly desirable. The CMOS compatibility is advantageous over the alternative approaches for ultra-violet sensors based on expensive high band gap materials such as GaN, AlGaN, and SiC as it is the only known approach to achieve economy of scale in mass production.

ACKNOWLEDGMENTS

This work was partially supported by the Focused Technology Area project on Nano Photonics for Detection and Sensing, funded by INNI and by the Kidron Fund. The devices were fabricated at the Micro Nano Fabrication Unit, Technion.

[1]V. Mikhelashvili, D. Cristea, B. Meyler, S. Yofis, Y. Shneider, G. Atiya, T. Cohen-Hyams, Y. Kauffmann, W. D. Kaplan, and G. Eisenstein, J. Appl. Phys. **116**, 074513 (2014).
[2]V. Mikhelashvili, D. Cristea, B. Meyler, S. Yofis, Y. Shneider, G. Atiya, T. Cohen-Hyams, Y. Kauffmann, W. D. Kaplan, and G. Eisenstein, J. Appl. Phys. **117**, 044503 (2015).
[3]S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[4]C. Lee, J. Meteer, C. Narayanan, and E. Kan, J. Electron. Mater. **34**, 1 (2005).
[5]S. Maikap, T.-Y. Wang, P.-J. Tzeng, C.-H. Lin, T. C. Tein, L. S. Lee, J.-R. Yang, and M. M.-J. Tsai, Appl. Phys. Lett. **90**, 262901 (2007).
[6]V. Mikhelashvili, B. Meyler, S. Yofis, Y. Shneider, A. Zeidler, M. Garbrecht, T. Cohen-Hyams, W. D. Kaplan, M. Lisiansky, Y. Roizin, J. Salzman, and G. Eisenstein, Appl. Phys. Lett. **98**, 212902 (2011).
[7]W. Banerjee, S. Maikap, T.-C. Tien, W.-C. Li, and J.-R. Yang, J. Appl. Phys. **110**, 074309 (2011).
[8]V. Mikhelashvili, B. Meyler, Y. Shneider, S. Yofis, J. Salzman, G. Atiya, T. Cohen-Hyams, G. Ankonina, W. D. Kaplan, M. Lisiansky, Y. Roizin, and G. Eisenstein, J. Appl. Phys. **113**, 074503 (2013).
[9]V. Mikhelashvili, B. Meyler, M. Garbrecht, S. Yofis, J. Salzman, T. Cohen-Hyams, W. D. Kaplan, Y. Roizin, M. Lisiansky, and G. Eisenstein, Appl. Phys. Lett. **98**, 022905 (2011).
[10]V. Mikhelashvili, Y. Shneider, B. Meyler, G. Atiya, S. Yofis, T. Cohen-Hyams, W. D. Kaplan, M. Lisiansky, Y. Roizin, J. Salzman, and G. Eisenstein, J. Appl. Phys. **112**, 024319 (2012).
[11]J. M. Lee and B. I. Kim, Mater. Sci. Eng. A **449–451**, 769 (2007).
[12]T. Aaltonen, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskela, Chem. Mater. **15**, 1924 (2003).
[13]L. Baker, A. S. Cavanagh, D. Seghete, S. M. George, A. J. M. Mackus, W. M. M. Kessel, Z. Y. Liu, and F. T. Wagner, J. Appl. Phys. **109**, 084333 (2011).
[14]C. Liu, C. C. Wang, C. C. Kei, Y. C. Hsueh, and T. P. Perng, Small **5**, 1535 (2009).
[15]S. J. Ding, H. B. Chen, X. M. Cui, S. Chen, Q. Q. Sun, P. Zhou, H. L. Lu, D. W. Zhang, and C. Shen, Nanoscale Res. Lett. **8**, 80 (2013).
[16]S. Novak, B. Lee, X. Yang, and V. Misra, J. Electrochem. Soc. **157**, H589 (2010).
[17]J. Chu, Z. Han, F. Meng, and Z. Wang, Solid-State Electron. **55**, 54 (2011).
[18]O. Bulteel, N. V. Overstraeten-Schlogel, A. Afzalian, P. Dupuis, S. Jeumont, L. Irenge, J. Ambroise, B. Macq, J.-L. Gala, and D. Flandre, in *Biomedical Engineering, Trends in Electronics, Communications and Software*, edited by A. N. Laskovski (InTech, 2011), Chap. 14, p. 257.
[19]M. Depas, B. Vermeire, P. W. Mertens, R. L. Van Meirhaeghe, and M. M. Heyns, Solid-State Electron. **38**, 1465 (1995).
[20]A. Stesmans and V. V. Afanas'ev, Appl. Phys. Lett. **82**, 4074 (2003).
[21]J. Robertson, Eur. Phys. J. Appl. Phys. **28**, 265–291 (2004).
[22]H. Zheng, Y. Zhou, and S. Gangopadhyay, J. Appl. Phys. **117**, 024504 (2015).

[23]M. Yun, B. Ramalingam, and S. Gangopadhyay, Nanotechnology **22**, 465201 (2011).
[24]V. Mikhelashvili, B. Meyler, M. Garbrecht, T. Cohen-Hyams, Y. Roizin, M. Lisiansky, W. D. Kaplan, Y. Salzman, and G. Eisenstein, Microelectron. Eng. **88**, 964 (2011).
[25]J. K. Kim, H. J. Cheong, Y. Kim, J.-Y. Yi, and H. J. Bark, Appl. Phys. Lett. **82**, 2527 (2003).
[26]A. Nakajima, H. Nakao, H. Ueno, T. Futatsugi, and N. Yokoyama, Appl. Phys. Lett. **73**, 1071 (1998).
[27]R. Tang, K. Huang, H. Lai, C. Li, Z. Wu, and J. Kang, Nanoscale Res. Lett. **8**, 368 (2013).
[28]X. Liang, J. Li, M. Yu, C. N. McMurray, J. L. Falconer, and A. W. Weimer, ACS Catal. **1**, 1162 (2011).
[29]J. Lu, B. Liu, J. P. Greeley, Z. Feng, J. A. Libera, Y. Lei, M. J. Bedzyk, P. C. Stair, and J. W. Elam, Chem. Mater. **24**, 2047 (2012).
[30]D. M. Fleetwood, "Border traps in MOS devices," IEEE Trans. Nucl. Sci. **39**, 269 (1992).
[31]P. Dianat, R. Prusak, A. Persano, A. Cola, F. Quaranta, and B. Nabet, IEEE Trans. Electron Devices **61**, 445 (2014).
[32]E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).
[33]H. P. Chen, Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, IEEE Trans. Electron Devices **59**, 2383 (2012).
[34]H. P. Chen, D. Veksler, G. Bersuker, and Y. Taur, IEEE Trans. Electron Devices **61**, 1483 (2014).
[35]F. Palumbo, P. Shekhter, and M. Eizenberg, Solid-State Electron. **93**, 56 (2014).
[36]M. A. Green and J. Shewhun, Solid-Slate Electron. **16**, 1141 (1973).
[37]P. S. Ho, E. S. Yang, H. L. Evans, and X. Wu, Phys. Rev. Lett. **56**, 177 (1986).
[38]J. Werner, A. F. Levi, R. T. Tung, M. Anzlowar, and M. Pinto, Phys. Rev. Lett. **60**, 53 (1988).
[39]P. Chattopadhyay and B. RayChaudhuri, Solid-State Electron. **35**, 1023 (1992).
[40]D. L. Scharfetter, Solid-State Electron. **8**, 299 (1965).
[41]P. Chattopadhyay and B. RayChaudhuri, Solid-State Electron. **36**, 605 (1993).
[42]L. Li, C. Richter, S. Paetel, T. Kopp, J. Mannhart, and R. C. Ashoori, Science **332**, 825 (2011).
[43]B. Skinner and B. I. Shklovskii, Phys. Rev. B **87**, 035409 (2013).
[44]P. Dianat, A. Persano, F. Quaranta, A. Cola, and B. Nabet, IEEE J. Sel. Top. Quantum Electron. **21**, 3800605 (2015).