IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Reduced common-mode voltage operation of a new seven-level hybrid multilevel inverter topology with a single DC voltage source

ISSN 1755-4535
Received on 23rd February 2015
Revised on 28th July 2015
Accepted on 31st July 2015
doi: 10.1049/iet-pel.2015.0130
www.ietdl.org

Arun Rahul Sanjeevan[1], R. Sudharshan Kaarthik[1], K. Gopakumar[1] ✉, P.P. Rajeevan[2], Jose I. Leon[3], Leopoldo G. Franquelo[3]

[1]*Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India*
[2]*Department of Avionics, Indian Institute of Space Science and Technology, Trivandrum, India*
[3]*Department of Electronics Engineering, University of Seville, Seville 41004, Spain*
✉ *E-mail: kgopa@cedt.iisc.ernet.in*

Abstract: In this study, analysis of extending the linear modulation range of a zero common-mode voltage (CMV) operated *n*-level inverter by allowing reduced CMV switching is presented. A new hybrid seven-level inverter topology with a single DC supply is also presented in this study and inverter operation for zero and reduced CMV is analysed. Each phase of the inverter is realised by cascading two three-level flying capacitor inverters with a half-bridge module in between. Proposed inverter topology is operated with zero CMV for modulation index <86% and is operated with a CMV magnitude of $V_{dc}/18$ to extend the modulation range up to 96%. Experimental results are presented for zero CMV operation and for reduced common voltage operation to extend the linear modulation range. A capacitor voltage balancing algorithm is designed utilising the pole voltage redundancies of the inverter, which works for every sampling instant to correct the capacitor voltage irrespective of load power factor and modulation index. The capacitor voltage balancing algorithm is tested for different modulation indices and for various transient conditions, to validate the proposed topology.

1 Introduction

Multilevel inverters are gaining popularity in medium- and high-voltage applications [1, 2]. By using multilevel inverters, drawbacks of two-level inverters such as electromagnetic interference, phase voltage distortion, switching losses, voltage stress on switching devices and high dv/dt can be mitigated to a great extent. On the contrary, multilevel inverters require complex power circuit topology, multiple DC power supplies, capacitors and a large number of switching devices. Main focus of development in multilevel inverter topologies is on reducing the number of switching devices, capacitors, DC power sources and developing associated pulse-width modulation (PWM) techniques [3–5].

Commonly used multilevel inverter topologies are neutral point clamped (NPC) inverters [6, 7], flying capacitor (FC) inverters [8–11] and cascaded H-bridge (CHB) inverters [12, 13]. By interconnecting these basic multilevel inverter topologies, hybrid multilevel inverter topologies can be derived [14–18]. The stacked multi-cell inverter presented in [19, 20] is an interesting topology with reduced switch voltage rating. Multilevel inverter topologies for open-end winding induction motor drives are another interesting area of research [21].

For a voltage source inverter fed induction motor drive system, the inverter pole voltage is the sum of motor phase voltage and common-mode voltage (CMV). In induction motors, there exists a parasitic capacitance between stator winding and stator iron, and between stator winding and rotor iron [22]. CMV with significant magnitude and high-frequency switching causes leakage current through these parasitic capacitances and motor bearings. This leakage current can cause flash over of bearing lubricant and corrosion of ball bearings, resulting in an early mechanical failure of the drive system [23, 24]. Another problem associated with this common-mode leakage current is the creation of electromagnetic interference on the drive control system [25]. One way to attenuate common-mode leakage current is by using bulky common-mode filters [26]. However, this scheme requires additional passive components making the system bulky and more expensive.

Another way of eliminating the CMV is by connecting the machine in an open-end winding configuration [27]. However, this scheme requires two isolated power supplies for operation. CMV elimination by modifying the PWM scheme for multilevel inverters with a single DC link is presented in [28–32].

In this paper, reduced CMV switching operation of a general *n*-level inverter by modifying the space vector (SV) switching technique is analysed. CMV eliminated operation [30–32] and reduced CMV operation of a new hybrid seven-level inverter topology with a single DC supply are also presented in this paper. The proposed inverter topology is operated with a zero CMV up to a linear modulation range of 86%. Operation of proposed inverter topology with reduced CMV ($V_{dc}/18$) using the new SV switching technique that results in extension of linear modulation range from 86 to 96% is presented in this paper. A hysteresis controller-based capacitor voltage balancing algorithm is implemented for controlling all the capacitor voltages. Due to the pole voltage redundancies of the proposed inverter topology, the capacitor voltages of the topology can be maintained towards the reference value irrespective of load power factor and the modulation index.

2 Inverter topology

Each phase of the proposed inverter is realised by cascading two three-level FC inverters, with a half-bridge module in between, as shown in Fig. 1. The topology consists of five pairs of complementary switches with 32 (2^5) switching states for each phase. In each phase, switches Sx1, Sx2, Sx3, Sx4, Sx5 and Sx1^, Sx2^, Sx3^, Sx4^, Sx5^, respectively ($x = a$, b, c phases) are operated in a complementary manner (Sx1 = 1 implies Sx1 is ON and Sx1^ is OFF). Each phase consists of three capacitors namely Cx1, Cx2 and Cx3, charged to voltages $V_{dc}/2$, $V_{dc}/3$ and $V_{dc}/6$, respectively. The first FC inverter (FC1) in Fig. 1 can generate

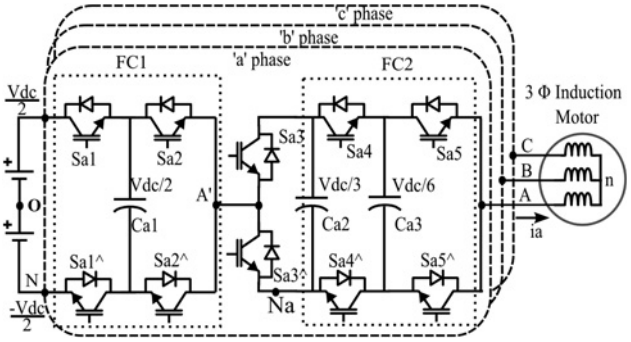

Fig. 1 *Power circuit for the proposed hybrid seven-level inverter topology with a single DC link. For the inverter topology, V_{AO} is defined as inverter pole voltage, V_{An} is defined as motor phase voltage and V_{nO} is defined as CMV*

voltage levels $-V_{dc}/2$, 0, $V_{dc}/2$ with respect to the DC bus midpoint 'O' and the second FC inverter (FC2) (Fig. 1) can generate voltage levels $V_{dc}/3$, $V_{dc}/6$, 0 with respect to 'N_a'. The two FC inverters are cascaded using a half-bridge module and this combination can generate pole voltage levels $-5V_{dc}/6$, $-2V_{dc}/3$, $-V_{dc}/2$, $-V_{dc}/3$, $-V_{dc}/6$, 0, $V_{dc}/6$, $V_{dc}/3$, $V_{dc}/6$, $2V_{dc}/3$ and $5V_{dc}/6$ with respect to the DC bus midpoint 'O'. Out of these 11 levels, $-5V_{dc}/6$, $-2V_{dc}/3$, $2V_{dc}/3$ and $5V_{dc}/6$ are not used as there are no switching state redundancies to maintain the capacitor voltages to its set value. Remaining seven pole voltage levels have switching state redundancies that can be used to correct the capacitor voltages towards the reference value in every switching cycle irrespective of the load power factor. Fig. 2 shows the redundant switching states and current path for pole voltage level $-V_{dc}/3$ for phase 'a'.

3 Common-mode eliminated states

The proposed inverter topology (Fig. 1) has 343 (7^3) pole voltage combinations. These pole voltage combinations can be mapped to 127 SV locations. Out of these, 37 pole voltage combinations have zero CMV ($V_{nO} = (V_{AO} + V_{BO} + V_{CO})/3$). These 37 SV locations form a SV structure similar to that of a four-level inverter rotated by 30° (Fig. 3*a*). Pole voltage combinations giving zero CMV for the shaded 60° region of seven-level SV structure in Fig. 3*a* is

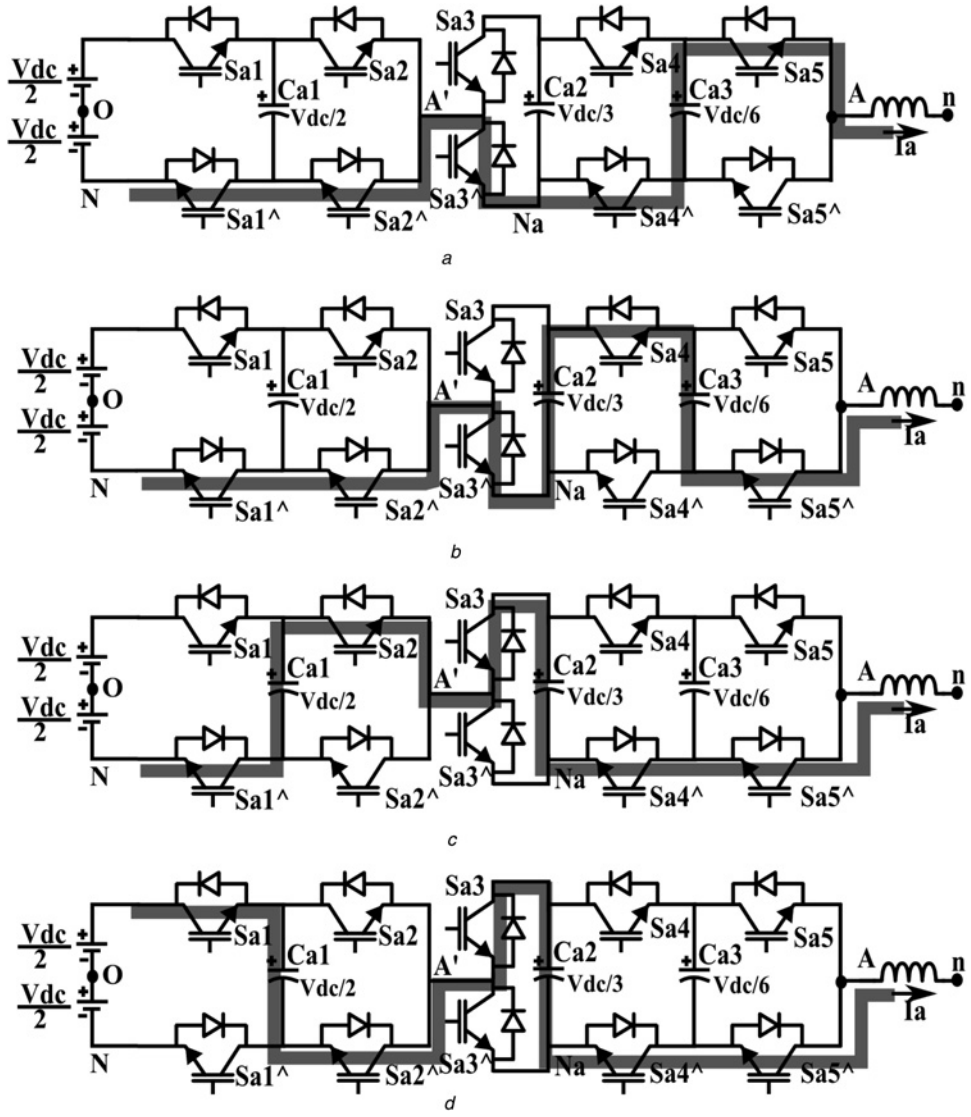

Fig. 2 *Switching states and current path for of pole voltage level $-V_{dc}/3$ for phase'a'*

a Current path for switch state of (0,0,0,0,1)
b Current path for switch state of (0,0,0,1,0)
c Current path for switch state of (0,1,1,0,0)
d Current path for switch state of (1,0,1,0,0)

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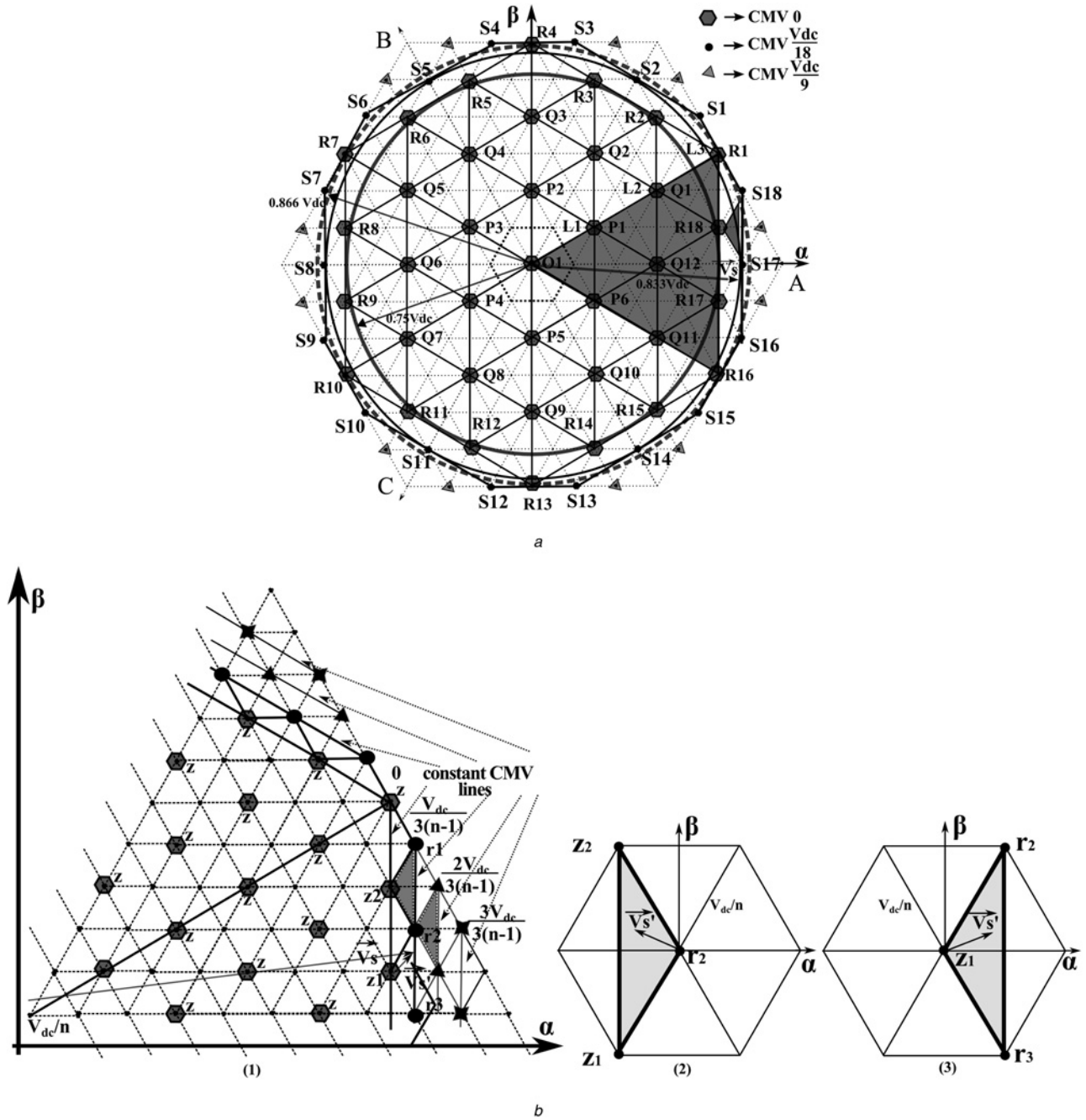

b

Fig. 3 *SV structure showing zero and reduced CMV SV locations*

a Four-level zero CMV SV structure is formed from a seven-level SV structure with three layers namely L1, L2 and L3. All the SV locations with CMV of $V_{dc}/18$ are marked (dark dots) as S1–S18

b (1) Sector 1 of a general *n*-level SV structure is showing zero CMV SV locations (marked as Z) and reduced CMV SV locations (dark dots). (2 and 3) Isosceles triangles formed by reduced CMV vectors are mapped to the inner hexagon of *n*-level SV structure for PWM timing calculation

explained in Table 1. From Fig. 3*a*, it can be seen that maximum radius of the circle inscribed by the seven-level SV structure (shown by dotted lines) is $0.866V_{dc}$ and radius of the circle inscribed by four-level SV structure is $0.75V_{dc}$, where V_{dc} is the radius of the seven-level SV hexagon. This means that with zero CMV operation, maximum linear modulation index possible is only 86%.

4 Extended linear modulation index operation with reduced CMV switching

For a general *n*-level inverter (where '*n*' is odd), there are $[(3/4)(n^2 - 1) + 1]$ (explained in Appendix) SV locations with zero CMV. By switching only the zero CMV SV locations, CMV of the inverter can be made zero. The disadvantage of this scheme is that the range of linear modulation index gets reduced. For any multilevel inverter, with SVPWM technique, peak of fundamental voltage possible is $0.577V_{dc}$ in the linear modulation range. If the same inverter is operated with zero CMV, peak of fundamental voltage reduces to $0.499V_{dc}$ ($0.866 \times 0.577\ V_{dc}$) in the linear modulation range. Hence, DC link voltage needs to be increased to maintain the drive torque capability for zero CMV operation. Another way to solve this reduction in linear modulation range is by allowing reduced CMV switching. The next smallest CMV magnitude is $(V_{dc}/3(n-1))$ and there are $3(n-1)$ such SV locations (shown as dark dots in Fig. 3*b*-1) for a general *n*-level inverter. Table 2 gives details of inverter operation with CMV swing between zero and $(V_{dc}/3(n-1))$ for the *n*-level inverter.

Table 1 Zero CMV SV locations of seven-level SV structure for 60° sector

Four-level SV location	Switching state combinations (V_{AO} level, V_{BO} level, V_{CO} level)	Zero CMV combination
O1	(−3,−3,−3), (−2,−2,−2), (−1,−1,−1), (0,0,0), (1,1,1), (2,2,2), (3,3,3)	(0,0,0)
P1	(−1,−2,−3), (0,−1,−2), (1,0,−1), (2,1,0), (3,2,1)	(1,0,−1)
P6	(−1,−3, −2), (0,−2,−1), (1,−1,0), (2,0,1), (3,1,2)	(1,−1,0)
Q1	(1,−1,−3), (2,0,−2), (3,1,−1)	(2,0,−2)
Q11	(1,−3,−1), (2,−2,0), (3,−1,1)	(2,−2,0)
Q12	(0,−3,−3), (1,−2,−2), (2,−1,−1)	(2,−1,−1)
R1	(3,0,−3)	(3,0,−3)
R16	(3,−3,0)	(3,−3,0)
R17	(2,−3,−2), (3,−2,−1)	(3,−2,−1)
R18	(2,−2,−3), (3,−1,−2)	(3,−1,−2)

Seven voltage levels $-V_{dc}/2$, $-V_{dc}/3$, $-V_{dc}/6$, 0, $V_{dc}/6$, $V_{dc}/3$, $V_{dc}/2$ are represented by −3, −2, −1, 0, 1, 2, 3

PWM timings for a general n-level inverter can be obtained by combining nearest CMV SV locations forming an isosceles triangle as shown in Fig. 3*b*-1. For PWM timing calculation, assume that reference voltage vector $\boldsymbol{V}_s$ falling in an isosceles triangle formed by SV locations z_1, r_2 and z_2 as shown in Fig. 3*b*-1. This isosceles triangle can be mapped to the inner hexagon of n-level SV structure as shown in Fig. 3*b*-2 (after mapping, $\boldsymbol{V}_s$ becomes$\boldsymbol{V}'_s$). Timings T_1, T_2 and T_0 for V_{z1}, V_{z2} and V_{r2} respectively, is calculated using $\boldsymbol{V}'_s$ as given in the following equation

$$T_1 = \frac{(n-1)T_s}{2V_{dc}}\left(\frac{V'_\alpha}{\cos(60^\circ)} - \frac{V'_\beta}{\sin(60^\circ)}\right)$$
$$T_2 = \frac{(n-1)T_s}{2V_{dc}}\left(\frac{V'_\alpha}{\cos(60^\circ)} + \frac{V'_\beta}{\sin(60^\circ)}\right) \quad (1)$$
$$T_0 = T_s - (T_1 + T_2)$$

where V'_α and V'_β are α and β axis components of reference voltage vector $\boldsymbol{V}'_s$ and T_s is the switching time period. Similarly, the isosceles triangle formed by the SV locations r_3, z_1 and r_2 (a mirror image of isosceles triangle z_1, r_2 and z_2) can be mapped to the inner hexagon as shown in Fig. 3*b*-3. PWM timings for vectors $\boldsymbol{V}_{r3}$, $\boldsymbol{V}_{r2}$ and $\boldsymbol{V}_{z1}$ can be calculated using (1). Likewise, PWM timing for all other isosceles triangles in all other sectors can be obtained.

In voltage source inverter fed induction motor drives, the induced shaft voltage and bearing current is proportional to the magnitude and frequency of CMV. In [33], it is shown that the average induced shaft voltage is around 1/25th of the CMV. With reduced CMV algorithm presented in this paper, with a CMV magnitude of $V_{dc}/18$ and with a reduced number of CMV switching, the induced shaft voltage will be less for the bearing oil breakdown to occur (breakdown voltage is around 8–15 V for PWM operation [34]).

Further increase in the linear modulation index is possible if the CMV switching from $(V_{dc}/3(n-1))$ to $(2V_{dc}/3(n-1))$ is allowed.

Table 3 Reduced CMV ($V_{dc}/18$) SV locations and switching state combinations are shown for a seven-level inverter

$V_{dc}/18$ SV locations	Switching state combinations	$V_{dc}/18$ SV locations	Switching state combinations
S1	(3,1,−3)	S10	(−3,−1,3)
S2	(2,2,−3)	S11	(−2,−2,3)
S3	(1,3,−3)	S12	(−1,−3,3)
S4	(−1,3,−3)	S13	(1,−3,3)
S5	(−2,3,−2)	S14	(2,−3,2)
S6	(−3,3.−1)	S15	(3,−3,1)
S7	(−3,3,1)	S16	(3,−3,−1)
S8	(−3,2,2)	S17	(3,−2,−2)
S9	(−3,1,3)	S18	(3,−1,−3)

It can be noted that the magnitude of CMV switching in this case is still $(V_{dc}/3(n-1))$. By switching the voltage vectors of isosceles triangle formed by the nearest CMV SV locations (Fig. 3*b*-1), the magnitude of CMV swing can be always made $(V_{dc}/3(n-1))$. By using this SV switching technique, full modulation range operation of 'n'-level inverter is possible with a CMV magnitude swing of $(V_{dc}/3(n-1))$. From Fig. 3*b*-1, for every isosceles triangle formed for SV PWM switching, two of the SV locations are always at same CMV. Hence, by using this SVPWM technique, frequency of CMV switching is also reduced. For n-level inverter, the dv/dt problems associated with increased CMV magnitude with high switching frequency can be reduced by using this SVPWM technique.

Fig. 3*a*, shows a seven-level SV diagram with all the SV locations having CMV of $V_{dc}/18$ (marked as S1–S18). Pole voltage combinations giving a CMV of $V_{dc}/18$ for these 18 SV locations are listed in Table 3. Linear modulation range of a seven-level inverter can be extended from 86 to 96% by allowing the CMV magnitude swing between zero and $V_{dc}/18$. For a seven-level inverter, full modulation index operation is possible if CMV switching of $V_{dc}/9$ to $V_{dc}/18$ is allowed (CMV magnitude swing is $V_{dc}/18$).

5 Capacitor voltage balancing

The inverter pole voltage levels, redundant switching states and effect of these switching states on capacitor charge are shown in Table 4 for phase 'a'. In the proposed inverter topology, all the capacitor voltages can be controlled towards the reference value in a switching cycle, irrespective of magnitude and direction of load current, by applying redundant inverter switching states. For a given pole voltage level, each capacitor can be charged or discharged properly by selecting a switching state from the available set of redundant switching states. It can be noted that (Table 4) for pole voltage levels $-V_{dc}/2$ and $V_{dc}/2$, the capacitor voltages are unaffected as all the capacitors are bypassed. For pole voltage levels $-V_{dc}/3$, 0 and $V_{dc}/3$ there are four redundant switching states, and for pole voltage levels $-V_{dc}/6$ and $V_{dc}/6$ there are five redundant switching states. These states along with hysteresis controllers are used for maintaining the capacitor

Table 2 Features of zero CMV and reduced CMV operations for n-level inverter are listed here

Inverter level (n) (n is odd)	Zero CMV SV structure level	Zero CMV SV locations	Next level reduced CMV magnitude	Reduced CMV SV locations	Maximum modulation index (m)	
					Zero CMV	CMV swings between zero and $\frac{V_{dc}}{3(n-1)}$
3	2	7	$V_{dc}/6$	6	0.8648	1
5	3	19	$V_{dc}/12$	12	0.8648	1
7	4	37	$V_{dc}/18$	18	0.8648	0.9627
9	5	61	$V_{dc}/24$	24	0.8648	0.9370
n	$\frac{n+1}{2}$	$\frac{3}{4}(n^2-1)+1$	$\frac{V_{dc}}{3(n-1)}$	$3(n-1)$	0.8648	$0.8648+\frac{1}{3(n-1)}$ with $(n \neq 3, 5)$

$m = 1$ corresponds to fundamental peak of $0.577V_{dc}$

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Table 4 Inverter switching states and effect on capacitor charging for phase '*a*'

Pole voltage (V_{AO})	Method of generation	Status of switches					Capacitor charging status					
							I_a + ve			I_a – ve		
		Sa1	Sa2	Sa3	Sa4	Sa5	Ca1	Ca2	Ca3	Ca1	Ca2	Ca3
$-V_{dc}/2$	$-V_{dc}/2$	0	0	0	0	0	U	U	U	U	U	U
	$-V_{dc}/2$	0	0	1	1	1	U	U	U	U	U	U
$-V_{dc}/3$	$-V_{dc}/2 + V_{dc}/6$	0	0	0	0	1	U	U	D	U	U	C
	$-V_{dc}/2 + V_{dc}/3 - V_{dc}/6$	0	0	0	1	0	U	D	C	U	C	D
	$-V_{dc}/2 + V_{dc}/2 - V_{dc}/3$	0	1	1	0	0	D	C	U	C	D	U
	$-V_{dc}/2 + V_{dc} - V_{dc}/2 - V_{dc}/3$	1	0	1	0	0	C	C	U	D	D	U
$-V_{dc}/6$	$-V_{dc}/2 + V_{dc}/3$	0	0	0	1	1	U	D	U	U	C	U
	$-V_{dc}/2 + V_{dc}/2 - V_{dc}/3 + V_{dc}/6$	0	1	1	0	1	D	C	D	C	D	C
	$-V_{dc}/2 + V_{dc}/2 - V_{dc}/6$	0	1	1	1	0	D	U	C	C	U	D
	$V_{dc}/2 - V_{dc}/2 - V_{dc}/3 + V_{dc}/6$	1	0	1	0	1	C	C	D	D	D	C
	$V_{dc}/2 - V_{dc}/2 - V_{dc}/6$	1	0	1	1	0	C	U	C	D	U	D
0	$-V_{dc}/2 + V_{dc}/2$	0	1	0	0	0	D	U	U	C	U	U
	$-V_{dc}/2 + V_{dc}/2$	0	1	1	1	1	D	U	U	C	U	U
	$V_{dc}/2 - V_{dc}/2$	1	0	0	0	0	C	U	U	D	U	U
	$V_{dc}/2 - V_{dc}/2$	1	0	1	1	1	C	U	U	D	U	U
$V_{dc}/6$	$-V_{dc}/2 + V_{dc}/2 + V_{dc}/6$	0	1	0	0	1	D	U	D	C	U	C
	$-V_{dc}/2 + V_{dc}/2 + V_{dc}/3 - V_{dc}/6$	0	1	0	1	0	D	D	C	C	C	D
	$V_{dc}/2 - V_{dc}/2 + V_{dc}/6$	1	0	0	0	1	C	U	D	D	U	C
	$V_{dc}/2 - V_{dc}/2 + V_{dc}/3 - V_{dc}/6$	1	0	0	1	0	C	D	C	D	C	D
	$V_{dc}/2 - V_{dc}/3$	1	1	1	0	0	U	C	U	U	D	U
$V_{dc}/3$	$-V_{dc}/2 + V_{dc}/2 + V_{dc}/3$	0	1	0	1	1	D	D	U	C	C	U
	$V_{dc}/2 - V_{dc}/2 + V_{dc}/3$	1	0	0	1	1	C	D	U	D	C	U
	$V_{dc}/2 - V_{dc}/3 + V_{dc}/6$	1	1	1	0	1	U	C	D	U	D	C
	$V_{dc}/2 - V_{dc}/6$	1	1	1	1	0	U	U	C	U	U	D
$V_{dc}/2$	$V_{dc}/2$	1	1	0	0	0	U	U	U	U	U	U
	$V_{dc}/2$	1	1	1	1	1	U	U	U	U	U	U

'U' – capacitor charge is unaffected, 'C' – capacitor is charging, 'D ' – capacitor is discharging and current flow from inverter pole '*A*' to machine neutral '*n*' is taken as positive

voltages to the reference value. The hysteresis controller output (H_{ai}) for capacitor voltage balancing for phase '*a*' can be defined as

$$H_{ai} = \begin{cases} 1, & V_{cai} \geq V_{cai}^* + \Delta V_{cai} \\ 0, & V_{cai} < V_{cai}^* - \Delta V_{cai} \end{cases} \quad (2)$$

where V_{cai} is *i*th capacitor voltage, V_{cai}^* is *i*th capacitor voltage reference, ΔV_{cai} is *i*th capacitor voltage ripple and $i = 1$, 2 and 3 for phase '*a*'. Hysteresis controller for other phases is identical.

Combining the hysteresis controller output for all three capacitors and current direction for each phase, a switching state selection table can be formed for all the pole voltage levels (Table 5) and is the same for all the phases. For example, in the present sampling instant for phase '*a*', let the inverter pole voltage level is $-V_{dc}/3$ and hysteresis controller output is ($I_{adir} = 0$, $H_{a1} = 0$, $H_{a2} = 0$, $H_{a3} = 0$). From Table 5, it can be concluded that all the capacitor voltages (V_{ca1}, V_{ca2} and V_{ca3}) are lower than the set value and require charging. There are four redundant switching states possible for the pole voltage of $-V_{dc}/3$ and switching state (1,0,1,0,0) will charge capacitors C_{a1} and C_{a2}, and C_{a3} will be unaffected. All other redundant switching states will discharge one of the capacitors furthermore. Hence, the switching state (1,0,1,0,0) is selected. Now set, inverter pole voltage to $-V_{dc}/6$ and hysteresis controller output is ($I_{adir} = 0$, $H_{a1} = 0$, $H_{a2} = 0$, $H_{a3} = 0$). The switching state selected for this condition is (1,0,1,1,0) and will charge capacitors C_{a1} and C_{a3}, and C_{a2} will be unaffected. Similarly, by using the above-mentioned hysteresis controller along with Table 5, switching state can be selected for all pole voltage levels to maintain each of the capacitor voltages at every sampling instant.

The capacitor voltage balancing control algorithm flowchart is shown in Fig. 4*a* for phase '*a*'. In the flowchart, hysteresis controller output forms the row index and level-data obtained from

Table 5 Switching state selection table based on capacitor voltage and current direction for phase '*a*'

I_{adir}	H_{a1}	H_{a2}	H_{a3}	Switching state selected (Sa1, Sa2, Sa3, Sa4, Sa5)				
				$-V_{dc}/3$	$-V_{dc}/6$	0	$V_{dc}/6$	$V_{dc}/3$
0	0	0	0	(1,0,1,0,0)	(1,0,1,1,0)	(1,0,0,0,0)	(1,1,1,0,0)	(1,1,1,1,0)
0	0	0	1	(1,0,1,0,0)	(1,0,1,0,1)	(1,0,0,0,0)	(1,0,0,0,1)	(1,1,1,0,1)
0	0	1	0	(0,0,0,1,0)	(0,0,0,1,1)	(1,0,0,0,0)	(1,0,0,1,0)	(1,0,0,1,1)
0	0	1	1	(0,0,0,0,1)	(0,0,0,1,1)	(1,0,0,0,0)	(1,0,0,0,1)	(1,0,0,1,1)
0	1	0	0	(0,1,1,0,0)	(0,1,1,1,0)	(0,1,1,1,1)	(1,1,1,0,0)	(1,1,1,1,0)
0	1	0	1	(0,1,1,0,0)	(0,1,1,0,1)	(0,1,1,1,1)	(1,1,1,0,0)	(1,1,1,0,1)
0	1	1	0	(0,0,0,1,0)	(0,1,1,1,0)	(0,1,1,1,1)	(0,1,0,1,0)	(0,1,0,1,1)
0	1	1	1	(0,0,0,0,1)	(0,0,0,1,1)	(0,1,1,1,1)	(0,1,0,0,1)	(0,1,0,1,1)
1	0	0	0	(0,0,0,0,1)	(0,0,0,1,1)	(0,1,1,1,1)	(0,1,0,0,1)	(0,1,0,1,1)
1	0	0	1	(0,0,0,1,0)	(0,1,1,1,0)	(0,1,1,1,1)	(0,1,0,0,1)	(0,1,0,1,1)
1	0	1	0	(0,1,1,0,0)	(0,1,1,0,1)	(0,1,1,1,1)	(1,1,1,0,0)	(1,1,1,0,1)
1	0	1	1	(0,1,1,0,0)	(0,1,1,1,0)	(0,1,1,1,1)	(1,1,1,0,0)	(1,1,1,1,0)
1	1	0	0	(0,0,0,0,1)	(0,0,0,1,1)	(1,0,0,0,0)	(1,0,0,0,1)	(1,0,0,1,1)
1	1	0	1	(0,0,0,1,0)	(1,0,1,1,0)	(1,0,0,0,0)	(1,0,0,1,0)	(1,0,0,1,1)
1	1	1	0	(0,0,0,0,1)	(1,0,1,0,1)	(1,0,0,0,0)	(1,0,0,0,1)	(1,1,1,0,1)
1	1	1	1	(1,0,1,0,0)	(1,0,1,1,0)	(1,0,0,0,0)	(1,1,1,0,0)	(1,1,1,1,0)

Let I_a is flowing from inverter pole '*A*' to motor neutral '*n*' as shown in Fig. 2, then $I_{adir} = 0$, else $I_{adir} = 1$

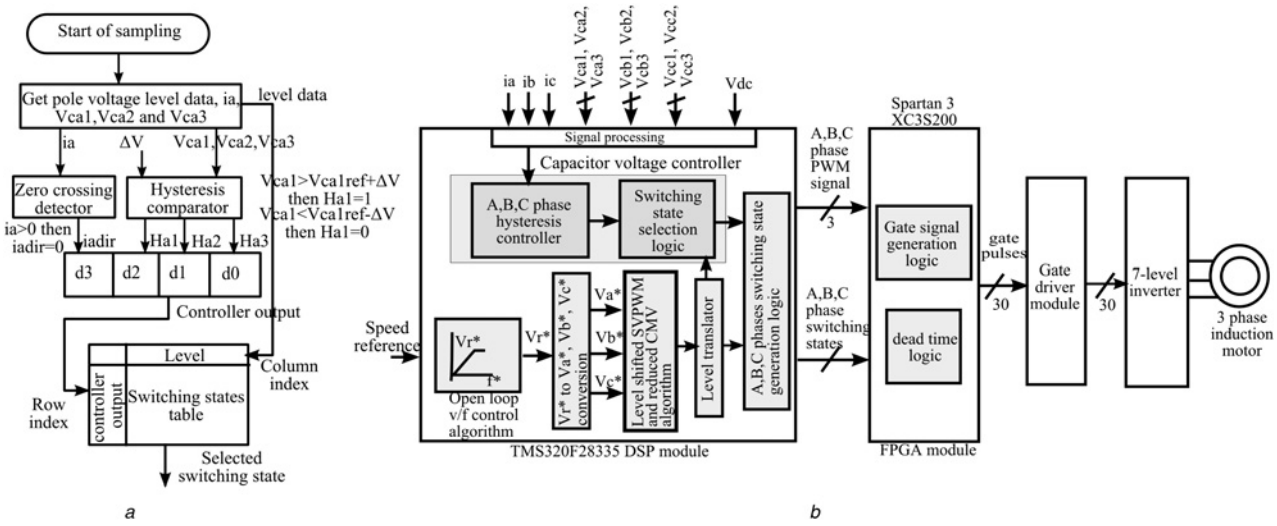

Fig. 4 *Flowchart of capacitor voltage controller; zero and reduced CMV operation implementation block diagram*

a Flowchart of capacitor voltage controller of '*A*' phase
b Zero and reduced CMV operation of inverter implementation block diagram

level shifted carrier-based PWM algorithm forms the column index for the switching state selection table (Table 5) for selecting the switching state. Similarly, for other phases also switching states to balance the capacitor voltage can be obtained.

6 Comparison with other inverter topologies

Proposed topology requires 12 insulated gate bipolar transistors (IGBTs) with voltage rating of $V_{dc}/2$, 6 IGBTs with voltage rating of $V_{dc}/3$ and 12 IGBTs with voltage rating of $V_{dc}/6$ with a total of 30 IGBTs. Number of capacitors required for the presented topology is given in Table 6. For the proposed topology, capacitor sizing can be made less compared with conventional topologies, because capacitor voltages can be corrected to the reference value, within a switching cycle, using the pole voltage redundancies. However, for a seven-level NPC and hybrid topology [35], there is a restriction in the modulation index with respect to the load power factor due to the capacitor voltage balancing problem. Comparison of the proposed inverter topology with other seven-level inverter topologies is shown in Table 6.

All the conventional inverter topologies can be operated with zero or reduced CMV algorithm presented in this paper. However, with a seven-level NPC inverter, additional algorithms must be needed for controlling the capacitor voltage fluctuations with the zero CMV operation. Moreover, capacitor voltage balancing depends on the load power factor and inverter modulation index. For over modulation operation also, capacitor voltages can be properly balanced in the proposed inverter topology, irrespective of the load power factor. With CHB inverters multiple isolated DC power supplies are required for zero CMV operation. Hence, the regenerative operation with CHB inverter will be a difficult task. Proposed inverter topology requires only a single DC power supply and can be effectively used for regenerative operation with zero or reduced CMV. A seven-level FC inverter is a good choice for zero or reduced CMV technique presented in this paper. The disadvantage with FC inverter is that it requires more number of semiconductor switches and capacitors compared with the proposed inverter topology. The capacitor sizing also will be higher for a FC inverter for a given voltage ripple and load current compared with the presented inverter topology.

7 Experimental results

Three-phase, 400 V, 3.7 kW, 50 Hz, two-pole induction motor drive with the open-loop V/f control scheme is implemented in the hardware for testing the proposed topology. TMS320F28335 digital signal processor (DSP) is used as the main controller and Xilinx SPARTAN-3 XC3S200 field programmable gate array (FPGA) as the PWM signal generator with dead time of 2.5 µs. Level shifted carrier-based PWM algorithm [36] is implemented for the zero CMV operation. PWM timing for reduced CMV operation is calculated using (1). To obtain the equivalent seven-level SV location from four-level SV location, a level translator algorithm is implemented. From the PWM algorithm, information about the pole voltage levels to be switched can be obtained for each phase. The presented capacitor voltage balancing algorithm requires only logical information of capacitor states. Low-cost operational amplifier (LM339)-based hysteresis controllers and zero crossing detectors are used for getting this logical information regarding the capacitor states and current direction. In the sampling period, for capacitor voltage balancing of each phase, the DSP selects a switching state using the capacitor voltage information, current direction and pole voltage data for each phase (Table 5). This switching state information along with the PWM timing data is sent to an FPGA module. The FPGA module generates the gating signals with a dead time of 2.5 µs for the gate driver module for all the three phases by processing the switching state information and PWM signals for the given sampling period. The implementation block diagram of zero and reduced CMV algorithm is shown in Fig. 4*b*.

A synchronous PWM technique is used for testing the inverter topology. Number of samples per sector is taken as ten for fundamental frequency ranging from 15 to 25 Hz, six for fundamental frequency ranging from 25 to 37.5 Hz and five for fundamental frequency ranging from 37.5 to 45 Hz. Inverter is operated with a constant switching frequency of 900 Hz for fundamental frequency below 15 Hz. The capacitor sizing is done by using the relation, $C = I_p/(f_s \times \Delta V_c)$, where C is the capacitance value of C_{a1}, C_{a2}, C_{a3}, C_{b1}, C_{b2}, C_{b3}, C_{c1}, C_{c2} and C_{c3}, I_p is the peak load current, ΔV_c is the peak-to-peak voltage ripple and f_s is the sampling frequency, which is twice the switching frequency. By considering 2.5 V peak-to-peak voltage ripple for all the capacitors and minimum sampling frequency (f_s) of 1800 Hz (twice the inverter switching frequency), capacitance value obtained is 1778 µF. For conducting the experiment, the capacitance value is selected as 2200 µF for all the three phases.

The proposed inverter can be operated with lower switching frequency, but the capacitor voltage ripple will be more for rated load current and it affects the voltage waveform quality at lower modulation index. With lower switching frequency, the inverter switching losses will be less but capacitor sizing needs to be increased for improving the voltage total harmonic distortion (THD).

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Table 6 Proposed inverter topology is compared with other seven-level inverter topologies

Inverter topology	Capacitor (V_{dc}/6)			IGBT			Clamping diodes	Power supplies	
	V_{dc}/2	V_{dc}/3	V_{dc}/6	V_{dc}/2	V_{dc}/3	V_{dc}/6		V_{dc}	V_{dc}/6
proposed topology	3	3	3	12	6	12	0	1	0
NPC	0	0	6	0	0	36	90	1	0
FC	0	0	45	0	0	36	0	1	0
CHB	0	0	0	0	0	36	0	0	9
hybrid topology [35]	0	0	9	0	18	24	0	1	0

In Fig. 5, inverter pole voltage for conventional SVPWM, zero CMV and reduced CMV operation is shown along with the frequency spectrum. Figs. 5*a* and *b* show the zero CMV and conventional SVPWM operation of inverter for a modulation index of 80%. From the frequency spectrum plot, it can be seen that zero CMV operation THD is better than conventional SVPWM operation THD. Figs. 5*c* and *d* show the reduced CMV and conventional SVPWM operation of inverter for a modulation index of 95%. The third harmonic component for reduced CMV operation is much less compared with conventional SVPWM operation. However, with zero CMV operation, inverter ΔV is $0.288V_{dc}$ $(0.866 \times 2V_{dc}/6)$ compared with $0.166V_{dc}$ for conventional SVPWM operation. Hence, switching loss is more compared with conventional SVPWM operation, but with zero CMV operation induced shaft voltages and bearing currents will be very less, which helps in improving the bearing life and reliability of the drive.

For testing the inverter topology, induction motor is run at frequencies 10 Hz [modulation index $(m) = 0.2$] with reference voltage vector tracing the region inside L1, 20 Hz ($m = 0.4$), 30 Hz

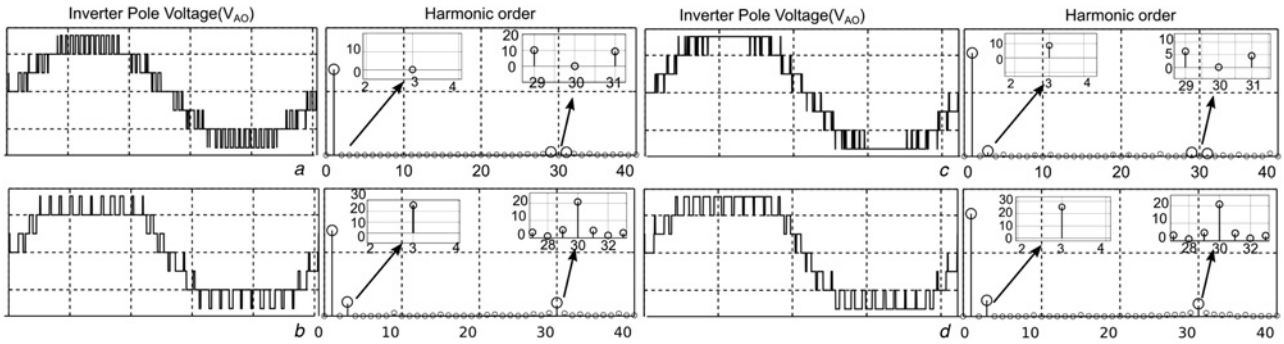

Fig. 5 *Inverter pole voltage (V_{AO}) and fast Fourier transform spectrum for zero CMV, reduced CMV and normal seven-level operation of inverter*

a Inverter pole voltage for zero CMV operation at a modulation index of 80%: *x*-axis = 4 ms/div, *y*-axis = 100 V/div
b Inverter pole voltage for conventional SVPWM operation at a modulation index of 80%: *x*-axis = 4 ms/div, *y*-axis = 100 V/div
c Inverter pole voltage for reduced CMV operation at a modulation index of 95%: *x*-axis = 5 ms/div, *y*-axis = 100 V/div
d Inverter pole voltage for conventional SVPWM operation at a modulation index of 95%: *x*-axis = 5 ms/div, *y*-axis = 100 V/div

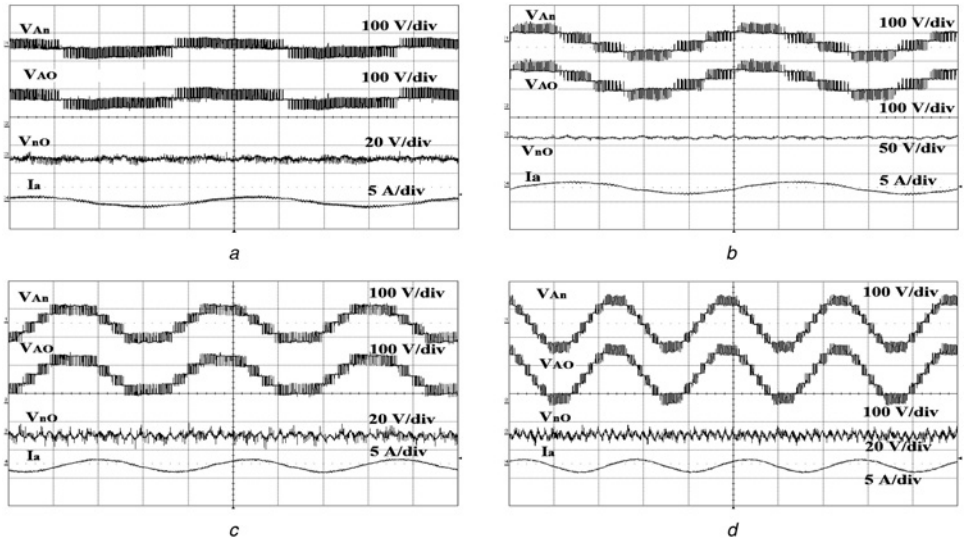

Fig. 6 *Experimental results show motor phase voltage (V_{An}), inverter pole voltage (V_{AO}),CMV (V_{nO}), phase current (I_a) for phase 'a' for different modulation index*

a 10 Hz operation with modulation index 0.2; Time scale: 20 ms/div
b 20 Hz operation with modulation index 0.4; Time scale: 10 ms/div
c 30 Hz operation with modulation index 0.6; Time scale: 10 ms/div
d 40 Hz operation with modulation index 0.8; Time scale: 10 ms/div

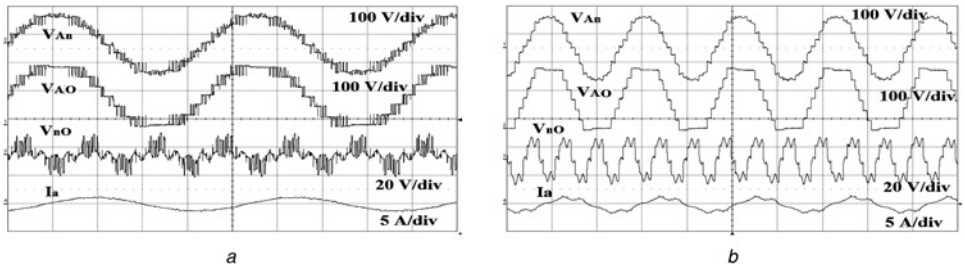

Fig. 7 *Experimental results show motor phase voltage (V_{An}), inverter pole voltage (V_{AO}), CMV (V_{nO}), phase current (I_a) for phase 'a' for different modulation index.*

a Extended modulation index ($m = 0.9$, frequency = 45 Hz) operation of the inverter with reduced CMV (DC bus voltage = 240 V). Time scale: 5 ms/div; *45 Hz with modulation index 0.9*
b Experimental results show over modulation operation with reduced CMV. In this mode of inverter operation, all the 24 SV locations on the asymmetric 12-sided polygon are switched one by one for equal duration. Time scale: 10 ms/div; *50 Hz with modulation index 1*

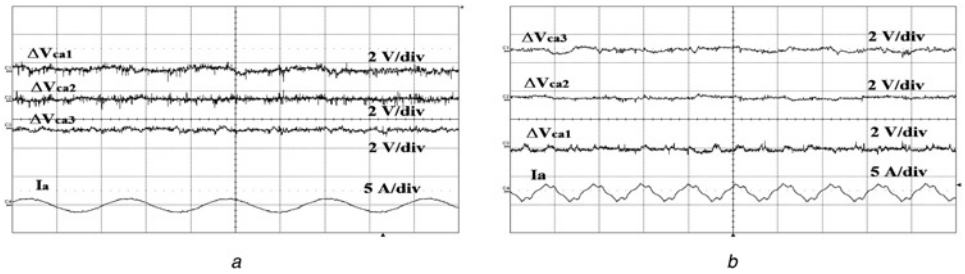

Fig. 8 *Experimental results show $V_{dc}/2$ capacitor voltage ripple (ΔV_{ca1}), $V_{dc}/3$ capacitor voltage ripple (ΔV_{ca2}), $V_{dc}/6$ capacitor voltage ripple (ΔV_{ca3}) and phase current (I_a) for phase 'a'*

a Capacitor voltage ripple for phase '*a*' is shown for extended modulation index ($m = 0.9$, 45 Hz) operation with reduced CMV. Time scale: 10 ms/div
b Capacitor voltage ripple for phase '*a*' is shown for 24-step operation of drive for modulation index (m) = 1 (tracing the SVs lying on 12-sided polygon). Time scale: 20 ms/div

($m = 0.6$) with reference voltage vector tracing the region between L1 and L2, 40 Hz ($m = 0.8$) with reference voltage vector tracing the region between L2 and L3 as shown in Fig. 3*a* at no load. Experimental results of these operations showing motor phase voltage (V_{An}), inverter pole voltage (V_{AO}),CMV (V_{nO}) along with phase current (I_a) for phase '*a*' are shown in Fig. 6. Inverter operation with CMV magnitude swinging between zero and $V_{dc}/18$ for a modulation index of 0.9 is shown in Fig. 7*a*. In Fig. 8*a*,

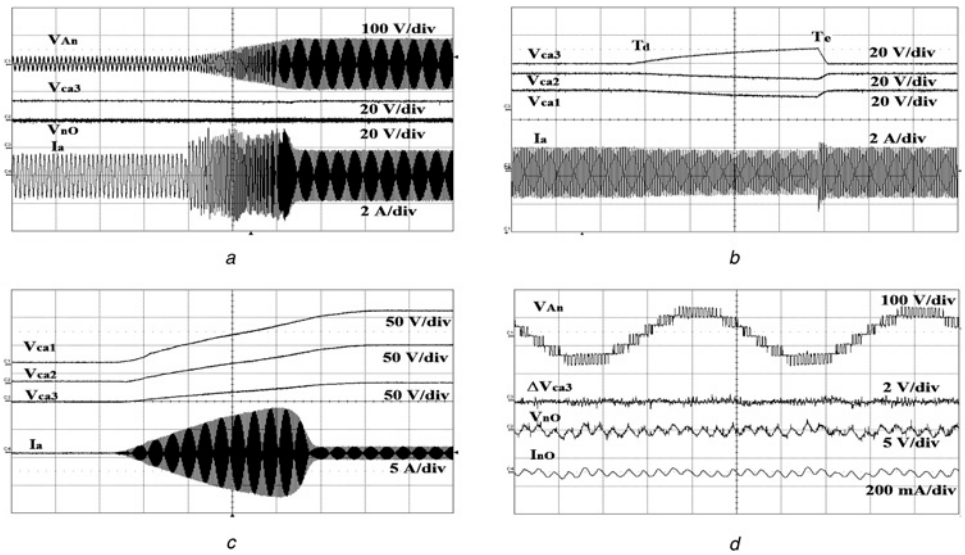

Fig. 9 *Experimental results show various operating conditions with zero CMV*

a Experimental results show sudden acceleration of motor from 10 to 40 Hz in 2.5 s. Waveforms shown are motor phase voltage (V_{An}), $V_{dc}/6$ capacitor voltage (V_{ca3}), CMV (V_{nO}) and phase current (I_a) for phase '*a*'. Time scale: 1 s/div
b Experimental results show the stability of capacitor voltage balancing algorithm. Capacitor voltage balancing algorithm is disabled at time T_d and again enabled at T_e. Wave forms shown are $V_{dc}/2$ capacitor voltage (V_{ca1}), $V_{dc}/3$ capacitor voltage (V_{ca2}), $V_{dc}/6$ capacitor voltage (V_{ca3}) and phase current (I_a). Time scale: 1 s/div.]
c Experimental results show charging of capacitor voltages to the reference voltage for phase '*a*' when inverter is switched on. Wave forms shown are $V_{dc}/2$ capacitor voltage (V_{ca1}), $V_{dc}/3$ capacitor voltage (V_{ca2}), $V_{dc}/6$ capacitor voltage (V_{ca3}) and phase current (I_a). Time scale: 1 s/div
d Experimental results show CMV eliminated operation of the inverter at 40 Hz by connecting a 10 Ω resistor between the neutral point '*n*' of induction motor and DC bus midpoint '*O*'. Waveforms shown are motor phase voltage (V_{An}), $V_{dc}/6$ capacitor voltage ripple (ΔV_{ca3}), CMV (V_{nO}), common-mode current (I_{nO}). Time scale: 5 ms/div

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capacitor voltage ripple for reduced CMV operation is shown. It can be noted that the capacitor voltages in all operations are well balanced.

By combining some of the zero CMV SV locations and all the reduced CMV SV locations, an asymmetric 12-sided SV polygon can be formed (Fig. 3*a*). Fig. 7*b* shows the experimental results of running the motor by applying all the voltage vectors of the asymmetric 12-sided polygon for equal duration at a modulation index of $m = 1$ ($f = 50$ Hz). Fig. 8*b* shows capacitor voltage ripple for the operation tracing all the voltage vectors lying on the asymmetric 12-sided polygon. Figs. 7*b* and 8*b* show that capacitor voltages are balanced across all operating conditions.

Fig. 9*a* shows the motor phase voltage (V_{An}), $V_{dc}/6$ capacitor voltage (V_{ca1}), CMV (V_{nO}) and machine current (I_a) for testing the acceleration of the motor from 10 to 40 Hz in 2.5 s. Fig. 9*c* shows all the three capacitor voltages building up when inverter is turned on. The stability of capacitor voltage balancing algorithm is tested by disabling the voltage balancing algorithm at time T_d and enabling at T_e. Fig. 9*b* shows that the capacitor voltages deviate from reference voltages at T_d and quickly come back to the reference voltages when balancing algorithm is enabled at T_e. To test the effectiveness of zero CMV operation, a resistor of 10 Ω is connected between the neutral point of induction motor to DC bus mid-point. Fig. 9*d* shows motor phase voltage (V_{An}), $V_{dc}/6$ capacitor voltage ripple (ΔV_{ca3}), CMV (V_{nO}) and common-mode current (I_{nO}) and it can be seen that CMV is <2 V and common-mode current is very negligible (<200 mA).

8 Conclusion

In this paper, a SVPWM technique is developed for a general *n*-level inverter with reduced CMV switching, which will make sure the CMV magnitude switching is always ($V_{dc}/3(n-1)$). By using this SVPWM technique, full linear modulation range operation of a general *n*-level inverter is possible with a magnitude of CMV swing ($V_{dc}/3(n-1)$).

In this paper, operation of a new hybrid seven-level inverter topology with zero CMV up to a modulation index of 86% is presented. The linear modulation index is extended to 96% by operating the inverter with CMV swing between zero and $V_{dc}/18$ by using the new SVPWM technique. By operating the inverter with CMV switching between $V_{dc}/9$ and $V_{dc}/18$, the linear modulation index can be extended to full range with CMV magnitude swing of $V_{dc}/18$.

The proposed topology is tested on a three-phase induction motor drive with open-loop V/f control scheme for various modulation indices and frequencies at no load and experimental results for steady-state operation is presented. Proposed inverter topology requires a lesser number of capacitors and switches than a FC inverter. During start-up of the converter, capacitors will automatically charge to the reference voltages by hysteresis controller and capacitor pre-charging circuitry is not required for the proposed topology. A hysteresis controller-based capacitor voltage balancing scheme is implemented for the inverter topology and tested for various fundamental frequencies at steady-state condition. Experimental results show that capacitor voltage balancing is obtained irrespective of the modulation index and load power factor. The stability of the capacitor voltage balancing algorithm is tested and validated experimentally by accelerating the motor, turning on the inverter at zero speeds, and temporarily disabling and then enabling the voltage balancing algorithm.

9 References

1 Rodriguez, J., Bernet, S., Wu, B., *et al.*: 'Multilevel voltage-source-converter topologies for industrial medium-voltage drives', *IEEE Trans. Ind. Electron.*, 2007, **54**, (6), pp. 2930–2945

2 Hatti, N., Hasegawa, K., Akagi, H.: 'A 6.6-kV transformer-less motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers', *IEEE Trans. Power Electron.*, 2009, **24**, (3), pp. 796–803

3 Kouro, S., Malinowski, M., Gopakumar, K., *et al.*: 'Recent advances and industrial applications of multilevel converters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (8), pp. 2553–2580

4 Abu-Rub, H., Holtz, J., Rodriguez, J., *et al.*: 'Medium-voltage multilevel converters – state of the art, challenges, and requirements in industrial applications', *IEEE Trans. Ind. Electron.*, 2010, **57**, (8), pp. 2581–2596

5 Malinowski, M., Gopakumar, K., Rodriguez, J., *et al.*: 'A survey on cascaded multilevel inverters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2197–2206

6 Nabae, A., Takahashi, I., Akagi, H.: 'A new neutral-point clamped PWM inverter', *IEEE Trans. Ind. Appl.*, 1981, **IA-17**, (5), pp. 518–523

7 Hasegawa, K., Akagi, H.: 'A new DC-voltage-balancing circuit including a single coupled inductor for a five-level diode-clamped PWM inverter', *IEEE Trans. Ind. Appl.*, 2011, **47**, (2), pp. 841–852

8 Amini, J.: 'An effortless space-vector-based modulation for N-level flying capacitor multilevel inverter with capacitor voltage balancing capability', *IEEE Trans. Power Electron.*, 2014, **29**, (11), pp. 6188–6195

9 Sadigh, A.K., Dargahi, V., Abarzadeh, M., *et al.*: 'Reduced DC voltage source flying capacitor multi-cell multilevel inverter: analysis and implementation', *IET Power Electron.*, 2013, **7**, (2), pp. 439–450

10 Choi, S., Saeedifard, M.: 'Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM', *IEEE Trans. Power Deliv.*, 2012, **27**, (3), pp. 1154–1161

11 Thielemans, S., Vyncke, T.J., Melkebeek, J.: 'Weight factor selection for model-based predictive control of a four-level flying-capacitor inverter', *IET Power Electron.*, 2012, **5**, (3), pp. 323–333

12 Villanueva, E., Correa, P., Rodríguez, J., *et al.*: 'Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems', *IEEE Trans. Ind. Electron.*, 2009, **56**, (11), pp. 4399–4406

13 Zha, X., Xiong, L., Gong, J., *et al.*: 'Cascaded multilevel converter for medium-voltage motor drive capable of regenerating with part of cells', *IET Power Electron.*, 2014, **7**, (5), pp. 1313–1320

14 Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H., *et al.*: 'New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels', *IET Power Electron.*, 2014, **7**, (1), pp. 96–104

15 Kangarlu, M.F., Babaei, E.: 'A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters', *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 625–636

16 Masaoud, A., Ping, H.W., Mekhilef, S., *et al.*: 'New three-phase multilevel inverter with reduced number of power electronic components', *IEEE Trans. Power Electron.*, 2014, **29**, (11), pp. 6018–6029

17 Mokhberdoran, A., Ajami, A.: 'Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology', *IEEE Trans. Power Electron.*, 2014, **29**, (12), pp. 6712–6724

18 Nami, A., Zare, F., Ghosh, A., *et al.*: 'A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode clamped H-bridge cells', *IEEE Trans. Power Electron.*, 2011, **26**, (1), pp. 51–65

19 Banaei, M.R., Oskuee, M.R.J., Kazemi, F.M.: 'Series H-bridge with stacked multicell inverter to quadruplicate voltage levels', *IET Power Electron.*, 2013, **6**, (5), pp. 878–884

20 Dargahi, S., Babaei, E., Eskandari, S., *et al.*: 'Flying-capacitor stacked multicell multilevel voltage source inverters: analysis and modelling', *IET Power Electron.*, 2014, **7**, (12), pp. 2969–2987

21 Mondal, G., Sivakumar, K., Ramchand, R., *et al.*: 'A dual seven-level inverter supply for an open-end winding induction motor drive', *IEEE Trans. Ind. Electron.*, 2009, **56**, (5), pp. 1665–1673

22 Chen, S., Lipo, T.A., Fitzgerald, D.: 'Source of induction motor bearing currents caused by PWM inverters', *IEEE Trans. Energy Convers.*, 1996, **11**, (1), pp. 25–32

23 Macdonald, D., Gray, W.: 'PWM drive related bearing failures', *IEEE Ind. Appl. Mag.*, 1999, **5**, (4), pp. 41–47

24 Busse, D., Erdman, J., Kerkman, R.J., *et al.*: 'Bearing currents and their relationship to PWM drives', *IEEE Trans. Power Electron.*, 1997, **12**, (2), pp. 243–252

25 Adabi, J., Zare, F., Ledwich, G., *et al.*: 'Leakage current and common mode voltage issues in modern AC drive systems'. Proc. of Australasian Universities Power Engineering Conf., December 9–12, 2007, pp. 1–6

26 Zhu, N., Kang, J., Xu, D., *et al.*: 'An integrated AC choke design for common-mode current suppression in neutral-connected power converter systems', *IEEE Trans. Power Electron.*, 2012, **27**, (3), pp. 1228–1236

27 Kanchan, R.S., Tekwani, P.N., Baiju, M.R., *et al.*: 'Three-level inverter configuration with common-mode voltage elimination for induction motor drive', *IEE Proc. Electr. Power Appl.*, 2005, **152**, (2), pp. 261–270

28 Cacciato, M., De Caro, S., Scarcella, G., *et al.*: 'Improved space-vector modulation technique for common mode currents reduction', *IET Power Electron.*, 2013, **6**, (7), pp. 1248–1256

29 Gupta, A.K., Khambadkone, A.M.: 'A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters', *IEEE Trans. Power Electron.*, 2007, **22**, (5), pp. 1672–1681

30 Rajeevan, P.P., Gopakumar, K.: 'A hybrid five-level inverter with common-mode voltage elimination having single voltage source for IM drive applications', *IEEE Trans. Ind. Appl.*, 2012, **48**, (6), pp. 2037–2047

31 Hoseini, S.K., Adabi, J., Sheikholeslami, A.: 'Predictive modulation schemes to reduce common-mode voltage in three-phase inverters-fed AC drive systems', *IET Power Electron.*, 2014, **7**, (4), pp. 840–849

32 Roshan Kumar, P., Rajeevan, P.P., Mathew, K., *et al.*: 'A three-level common-mode voltage eliminated inverter with single DC supply using flying capacitor inverter and cascaded H-bridge', *IEEE Trans. Power Electron.*, 2014, **29**, (3), pp. 1402–1409

33 Naik, R., Nondahl, T.A., Melfi, M.J., *et al.*: 'Circuit model for shaft voltage prediction in induction motors fed by PWM-based AC drives', *IEEE Trans. Ind. Appl.*, 2003, **39**, (5), pp. 1294–1299

34 Erdman, J., Kerkman, R.J., Schlegel, D., *et al.*: 'Effect of PWM inverters on AC motor bearing currents and shaft voltages'. Tenth Annual Conf. Proc. of Applied

Power Electronics Conf. and Exposition, APEC '95, 1995, 1995, 5–9 March 1995, vol. 1, pp. 24–33
35 Saeedifard, M., Barbosa, P.M., Steimer, P.K.: 'Operation and control of a hybrid seven-level converter', *IEEE Trans. Power Electron.*, 2012, **27**, (2), pp. 652–660
36 Kanchan, R.S., Baiju, M.R., Mohapatra, K.K., *et al.*: 'Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages', *IEE Proc. Electr. Power Appl.*, 2005, **152**, (2), pp. 297–309

10 Appendix

(i) For 'n'-level inverter number of concentric hexagons = $(n-1)$
(ii) For 'n- level inverter number of SV locations in the outermost hexagon = $6(n-1)$
(iii) For 'n'-level inverter number of SV locations in the next innermost hexagon = $6(n-2)$
(iv) Number of SV locations for 'n'-level inverter can be calculated as given below.

$$\begin{aligned}&\text{Total space vector locations}\\&= 6[(n-1)+(n-2)+\cdots+(n-(n-1))]+1\\&= 3[(n-1)+(n-(n-1)](n-1)+1\\&= 3[n(n-1)]+1\end{aligned}$$

(v) Zero CMV SV structure level possible from 'n'-level inverter (n is odd) = $((n+1)/2)$
(vi) Total zero CMV SV locations = $[(3/4)(n^2-1)+1]$
(vii) Let a, b and c phases of 'n'-level inverter be at voltage levels n_a, n_b and n_c then, CMV $V_{nO} = ((V_{dc}(n_a+n_b+n_c))/3(n-1))$

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